Asynchronous wired-logic control

- Context:
  - we’ve examined synchronous
    - wired logic
    - microprogrammed

Asynchronous wired-logic control

- Ideas

- asynchronous =>
  - no clock
  - every gate (Muller model) or every feedback loop (Huffman model) has a pure, positive delay

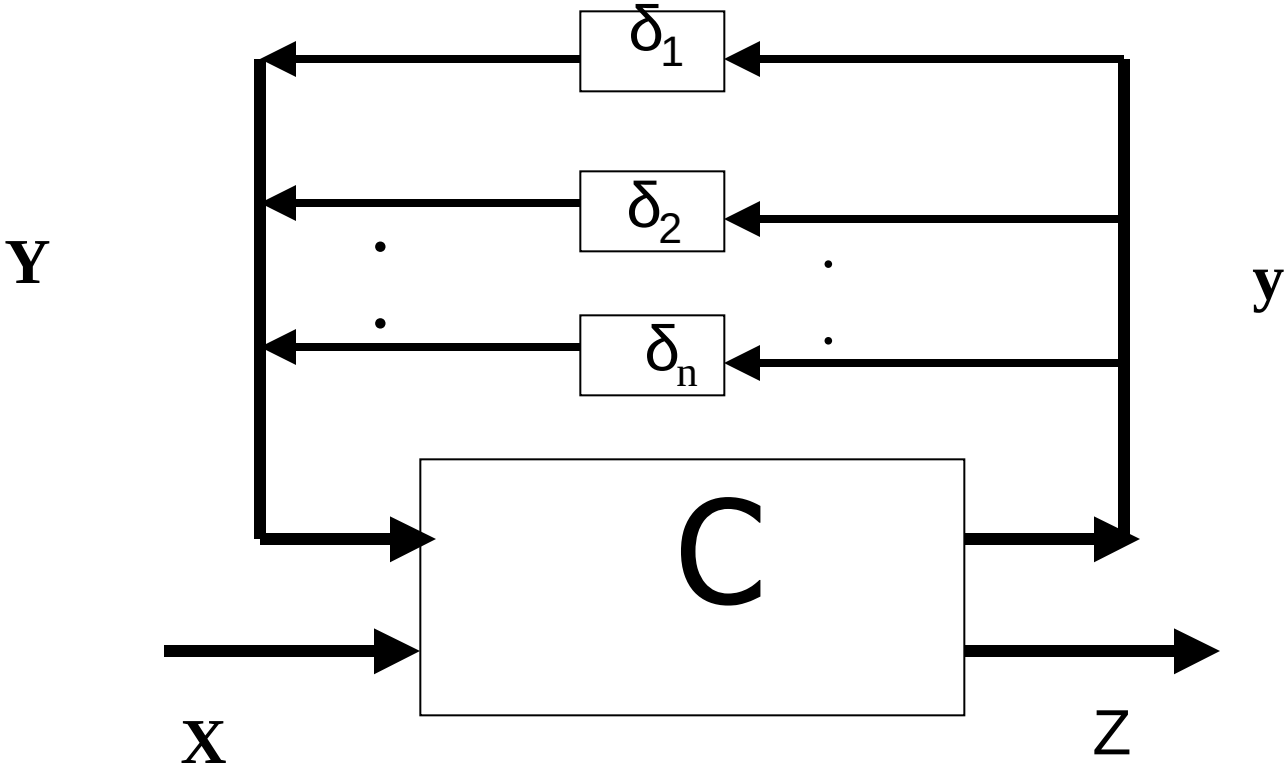
Asynchronous ==>

– circuit must have the same behaviour
independent of all possible changes in delays

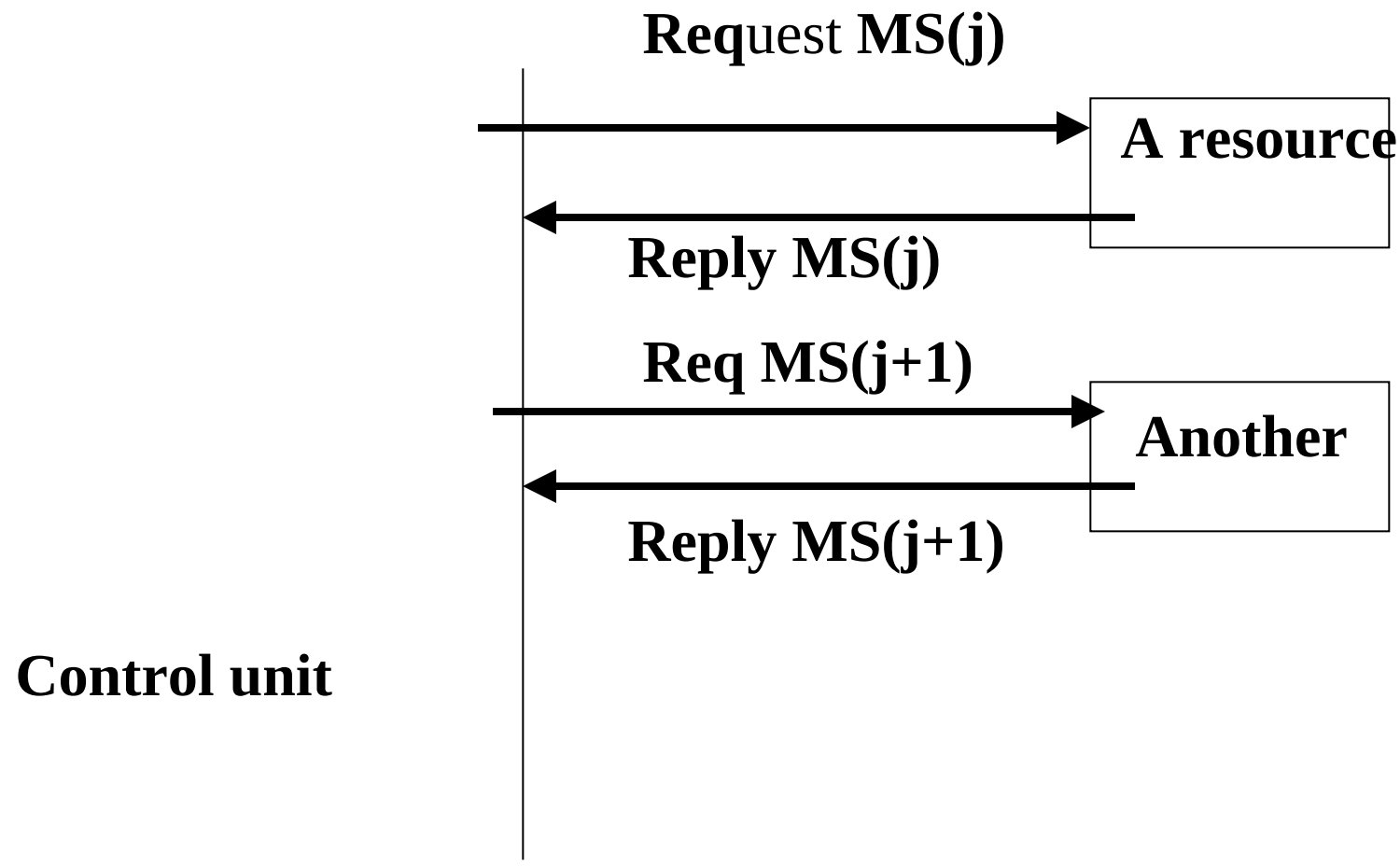
– no critical races

– no oscillations

Huffman Model

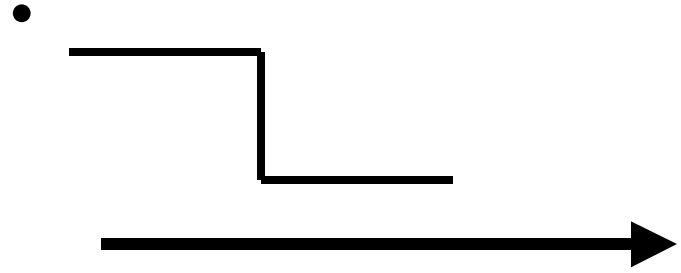


Control setup

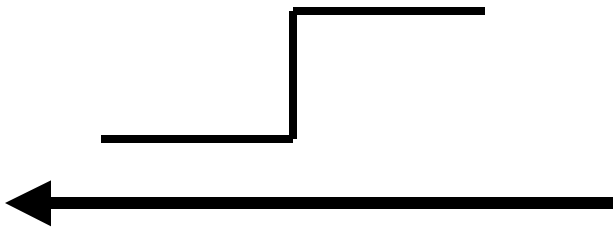


Protocol between control & resources

- 1] Request MS (j)
- 2] MS(j) begins

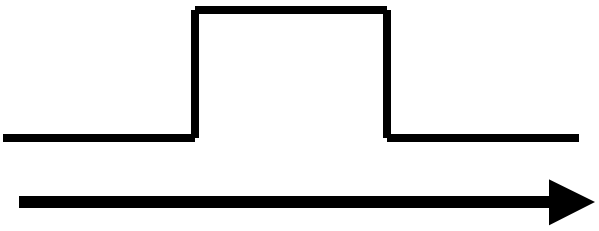


- 3] Reply “ it’s done”

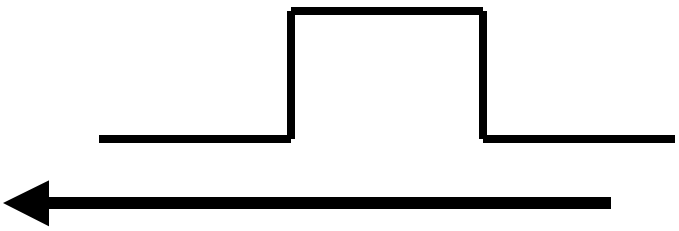


Protocol

- 4] Reply heard: turn off Request



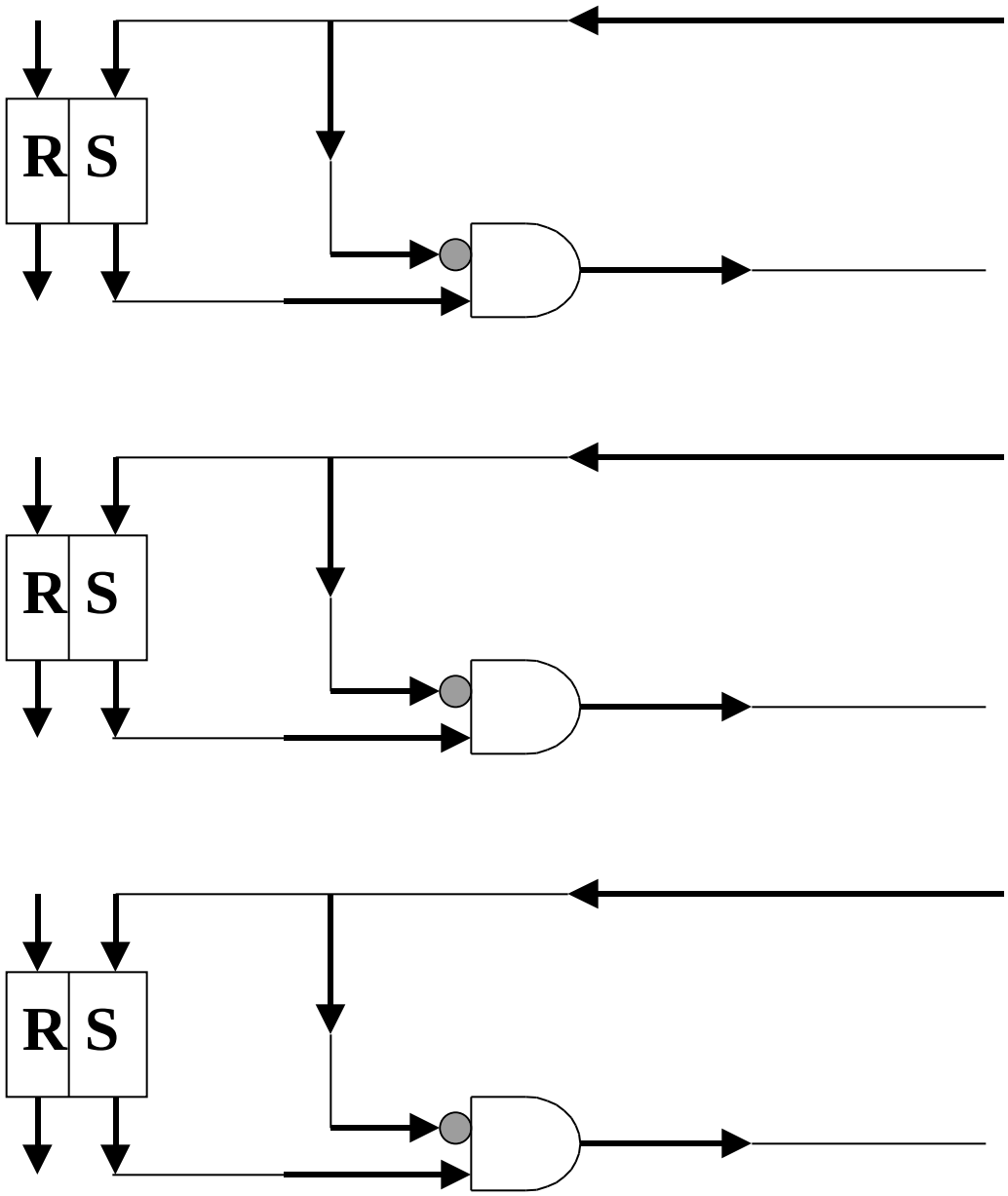
- 5] Request heard off: turn off Reply



- 6] Reply heard off: start Request MS(j+1)

NB

- Functions correctly, independent of microstep duration
- no clock
- each resource (ALU, register, bus, . . .) must generate a true reply.
- How to design the control??
  - Using 1-active SR flipflops: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