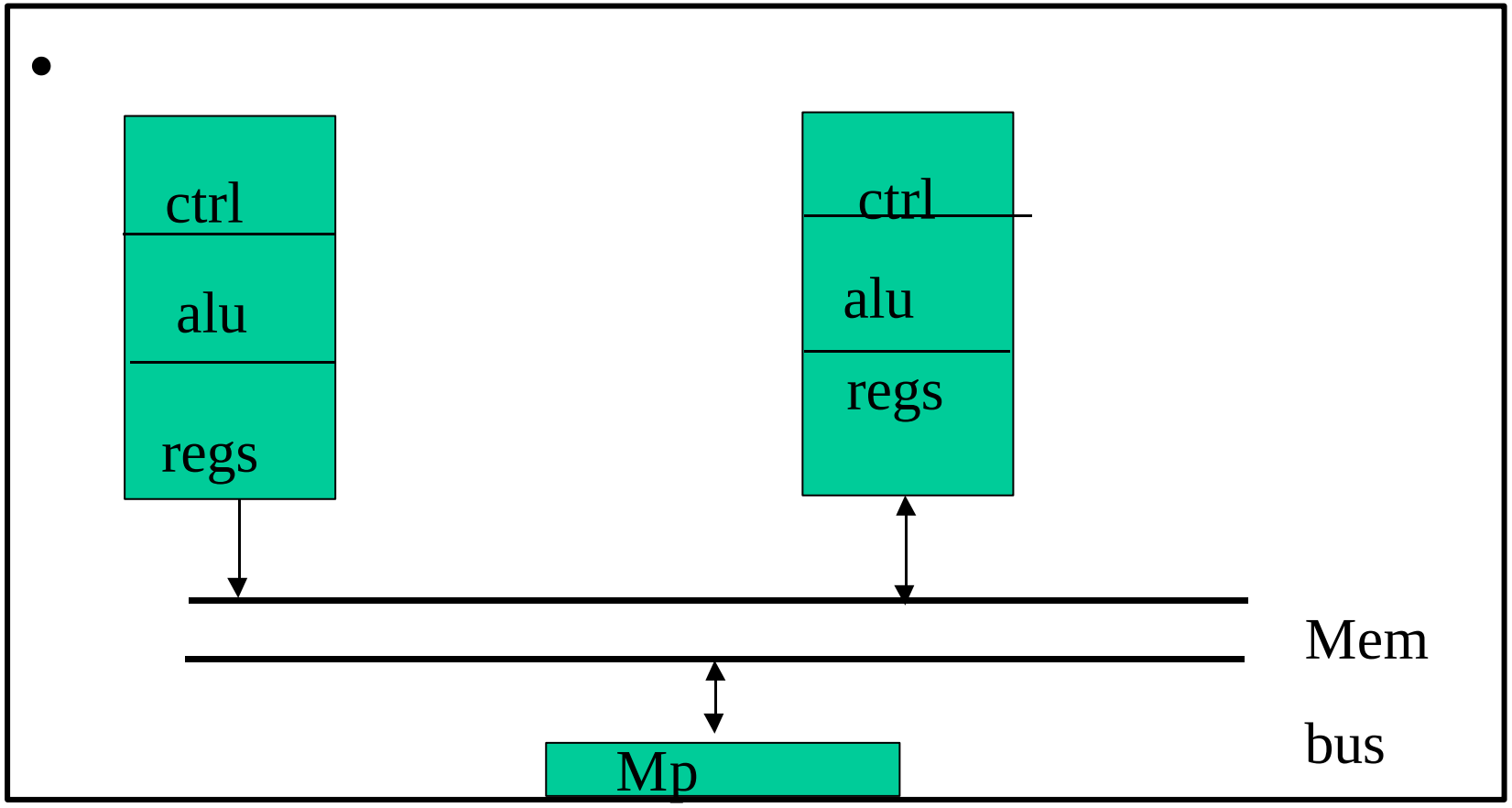
Types of machines
Flynn's Taxonomy

- 1] sequential -- one instruction at a time -- or SISD
- 2] to go faster -- Parallel Machines.

  - Types
    - Single Instruction Multiple Data stream (SIMD)
    - Multiple Instruction Multiple Data stream (MIMD)
    - Multiple Instruction Single Data stream (MISD)
    - Single Instruction SIngle Data stream (SISD)

    - see PH Chapter 9

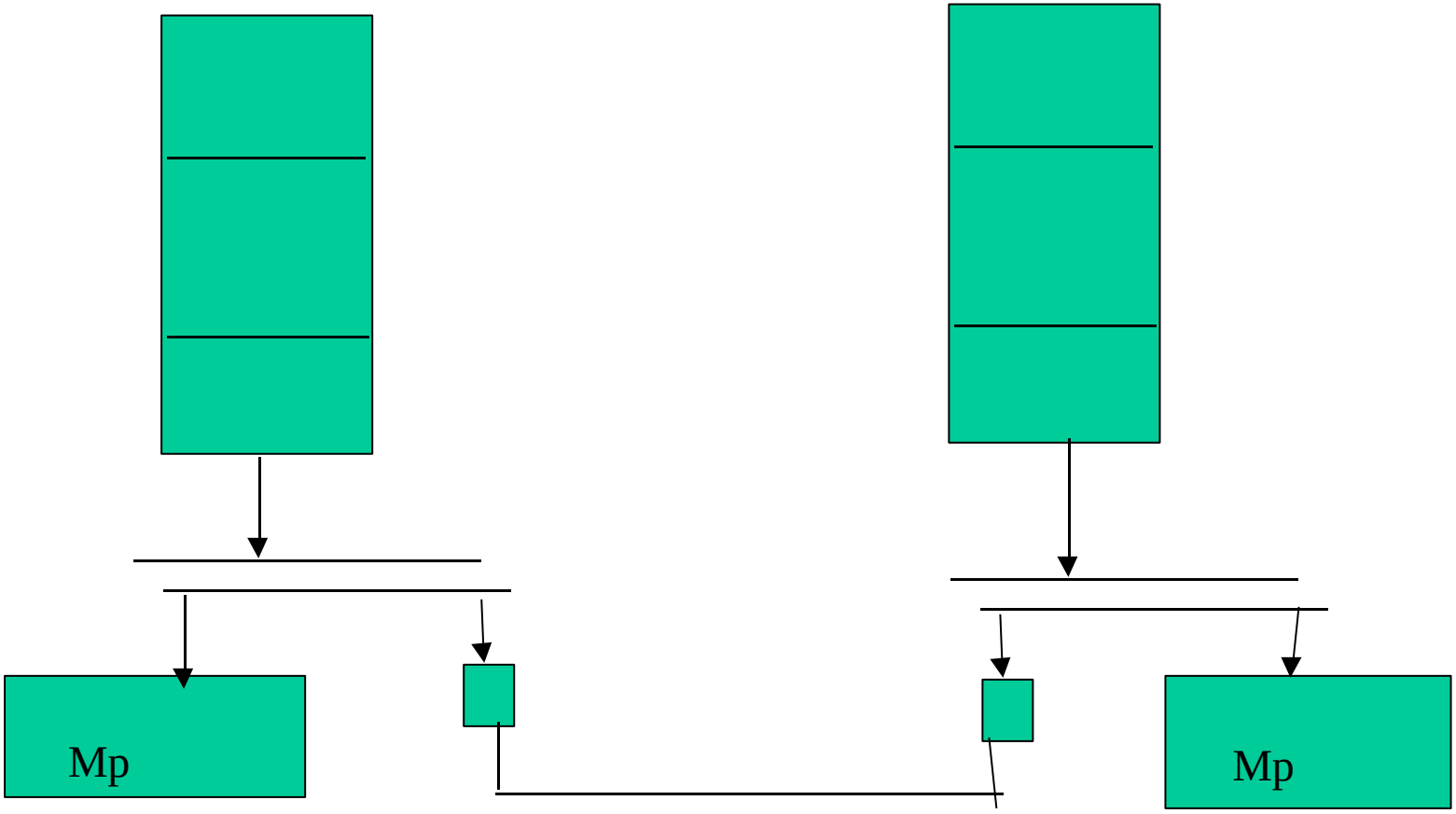
MIMD example: shared-memory multiprocessors



MIMD

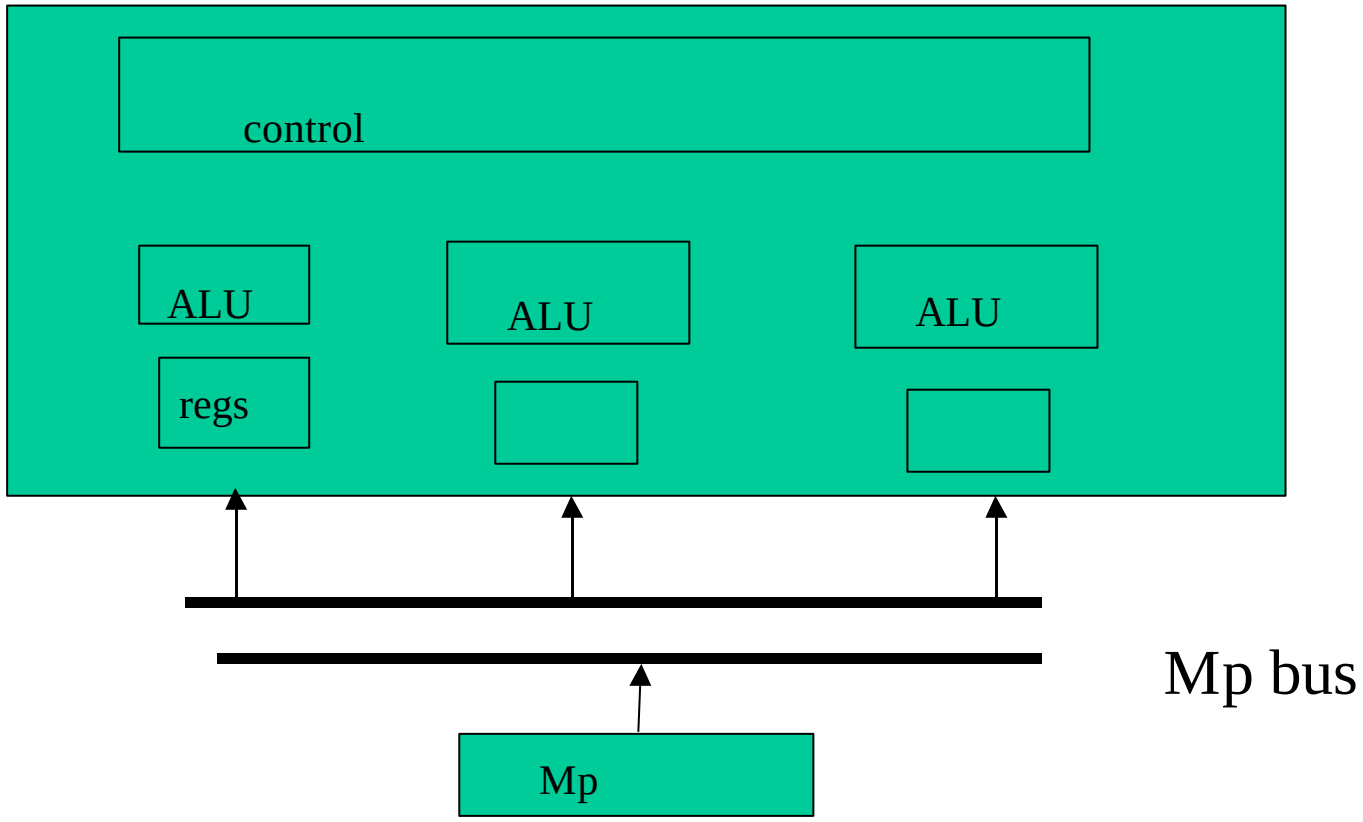
- above is a tightly-coupled (shared-memory) multiprocessor

Loosely-coupled MIMD



- Machines connected via the InterNet??

SIMD

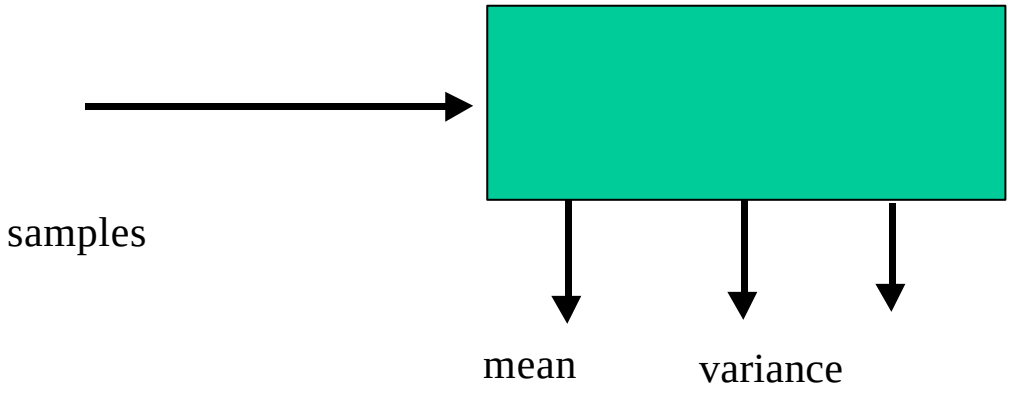
- 

SIMD

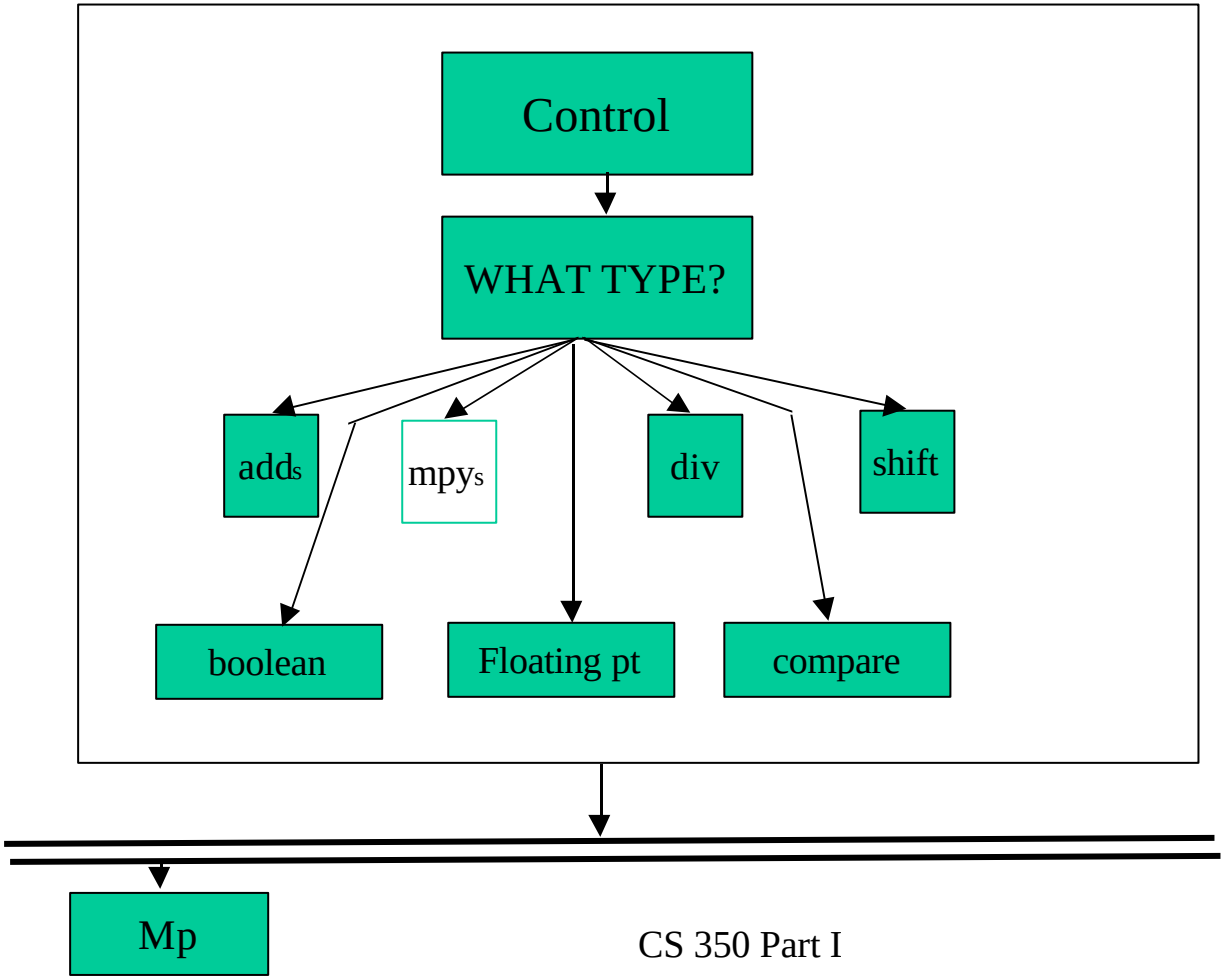
- Example : ILLIAC IV
- programming problems??

MISD

- Even more exotic
- moments of a distribution in real time



SISD,
MULTIFUNCTIONAL



Examples

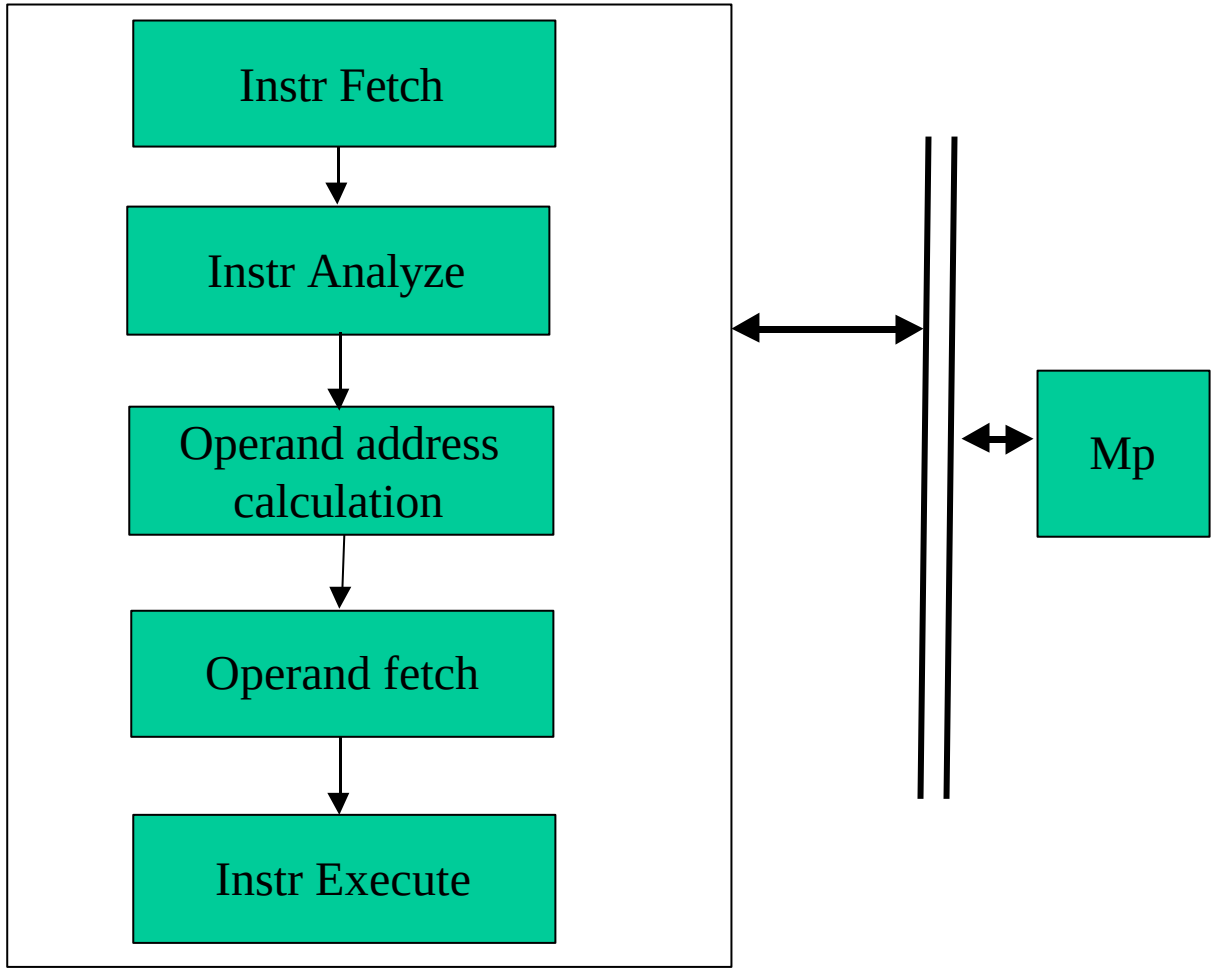
- Control Data / Cray Research / Silcon Graphics supercomputers

- Question: any multifunctional microprocessors??

SISD: Pipelined

-

P-H CH 6



SISD: Pipelined

- Examples:
  - MIPS chip
  - most modern microprocessors
- Is there parallelism?

- Combine with the previous slide for higher performance

Pipelining

can be done at other levels too . . .

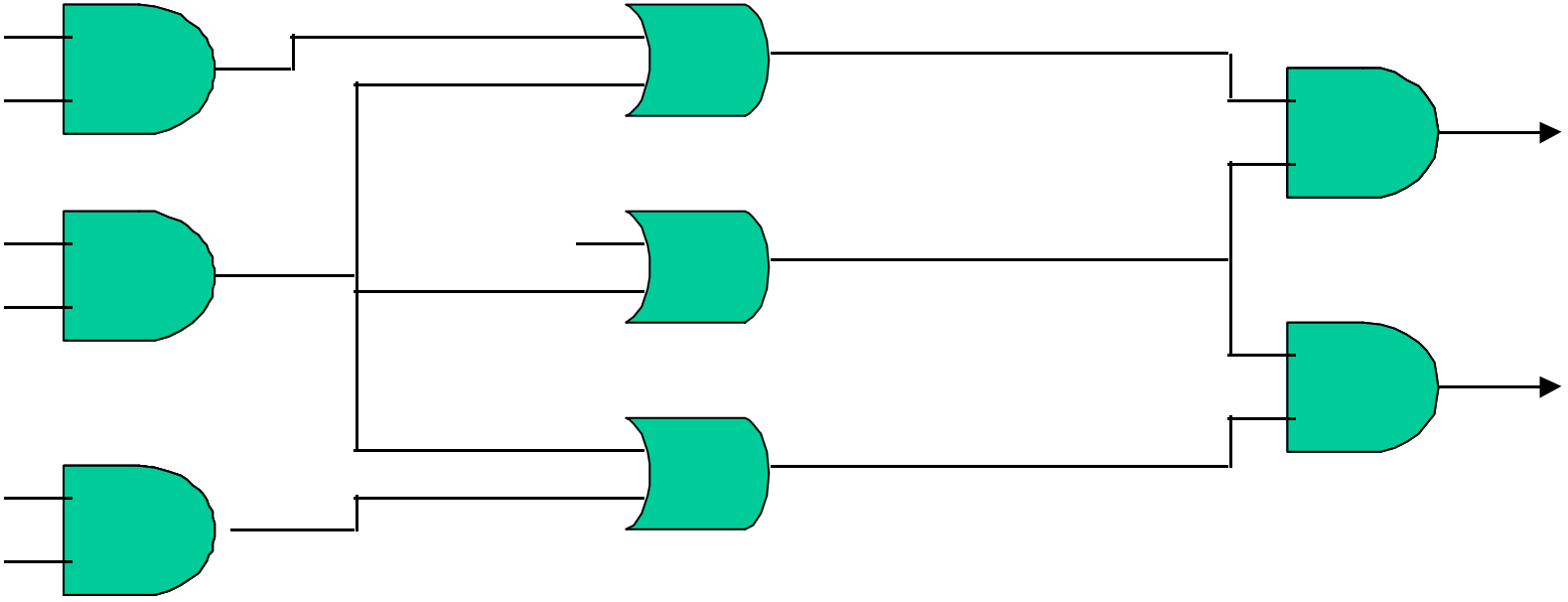
Consider the combinational gate network

$D_g = \tau$

$D_s = 3\tau$

($n\tau$ for n levels)

$R = 1/ 3\tau$

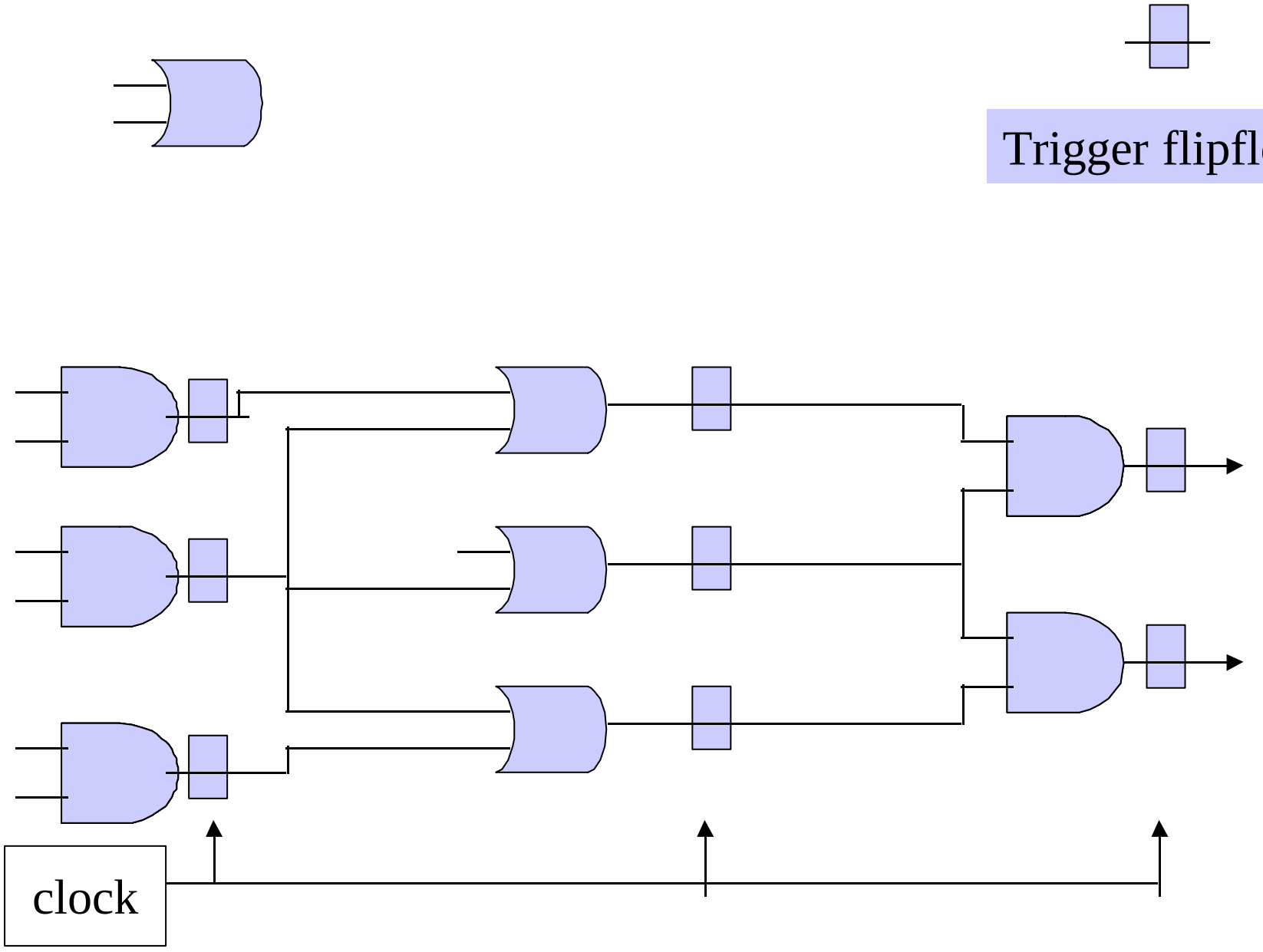


Level 1 Level 2 Level 3

Operation:

- Apply X
- WAIT until new signals have propagated through all levels of logic and created stable new outputs Z (how long??)
- Apply new X and repeat . . .

How to pipeline ??


Trigger flipflop
clock

Operation

- Apply X
- WAIT until ???
- Apply new X . . .

* Fresh values of **X** fed in at intervals of $\tau + \delta$
(δ = flipflop delay)

$D_s = \tau + \delta$ (the same for n levels)

$R = 1/(\tau + \delta)$ (the same for n levels)

* But each **X** requires

$n(\tau + \delta)$

to get thru the circuit

(i.e. to generate its output vector **Z**)

Turbulence in pipes, or stalls

- What happens to the pipelined CPU when

  An interrupt or
  a conditional jump occurs??

Is a pipelined CPU good for timesharing?

Hybrids:

Multifunction and pipelining can be combined – often are

- Some real pipelined machines

  IBM 360/91 (1969, $ 10 million)

  CDC Star

  MOS Technology 6502 (1975, $100)

  MOS 6502 had instr and data fetch boxes, and instruction execute box

Pipelined: MIPS R 2000, R 3000, R 4000 (1995, $500)
Part II of this course!