Primary Memory
M_p

Conventional memory

A sequence of *cells* with *names*

0
1
2
.
.
.
n

Primary Memory
M_p

cell Y also has a *content* c(Y)

which has NO relationship to its name

c(Y) is a string of bits

L(c(Y)) is defined to be the *word size or cell size*

Primary Memory
M_p

Cells are *randomly accessible* i.e.

Cell Access time

T_{access}

is constant for all cells and for all sequenc
of cell accesses (unlike disc or tape)

Values of Cell Length:

L(c(Y)) =

1	Burroughs 1700 (bit-addressable!)
8	IBM 1401 (byte-addressable
8 & 16	DEC pdp-11 (byte & word-addressable)
8 & 32	MIPS R4000, IBM 370, Motorola M68000

Values of Cell Length:

12	DEC pdp-12
18	DEC pdp-15
36	Honeywell Series 60
60	CDC Cyber 70

What's going on here?

- Early machines were for *scientific* applications =>
  Cell-lengths of 36, 48, 60 bits

- Later machines (S/ 360, pdp-11, M 68 000) were fo

  Scientific => long cells *and*
  Character-manipulating => 8-bit cell (byte

  Applications

Digression about addressability

- byte-addressability and larger memories (10^8 total b instead of 10^6 total bits) imply

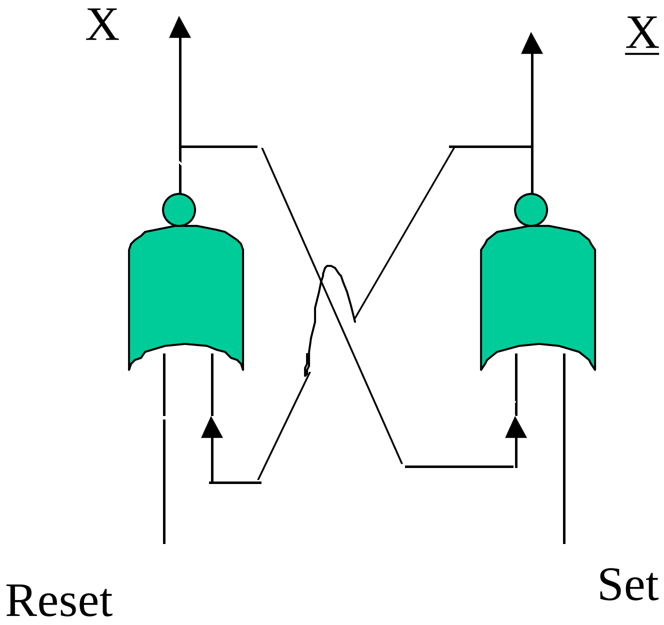
- many more cells
  (10^6 cells instead of 10^4) which implies

- much larger real address spaces: 24- 48 bits instead 16 bits which implies

Digression about addressability

- addresses cannot be kept in instructions : the addres length is greater than the instruction length!
- See MIPS chip for the solution

How to Build Primary Memory?

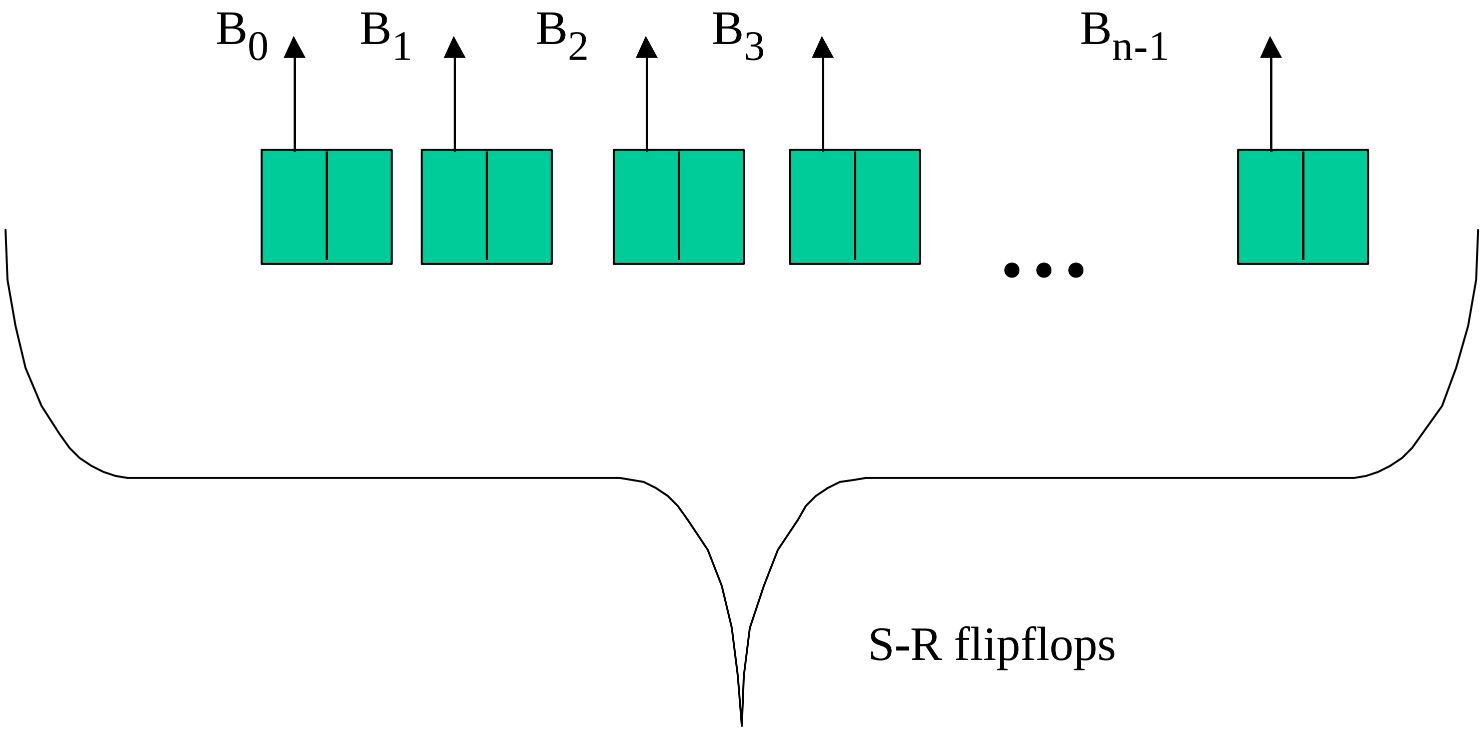


S	R	X	state
1	0	1	SET
0	1	0	RESET
0	0	?	REMEMBER
1	1		NO - NO

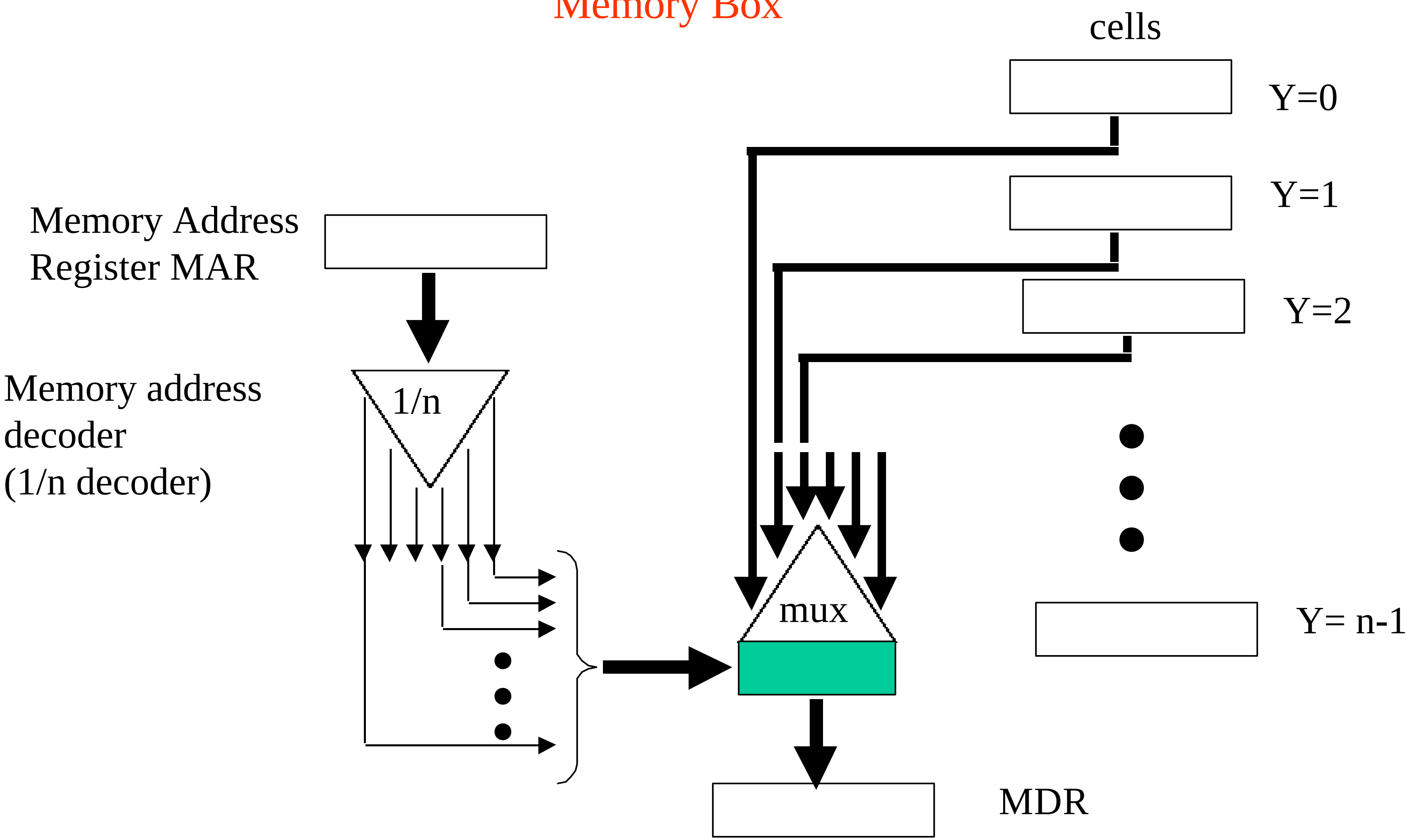
SET = storing 1
RESET = storing 0

1- Acting NOR-implemented SET-RESET flipflop

Primary Memory II
Making A Cell



Primary Memory III
Memory Box



Primary Memory IV
Specification

Primary Memory V
Prices & Sizes

1967:

1 cent per bit ==> $800 000 per megabyte
mainframes: 1 or 2 Mbytes
magnetic cores

1979:

16K SR flipflops per chip (16K RAM)
$30 per chip or 0.2 cents/bit
mainframes: 8 Mbytes
PCs: 128Kb -- 512 Kbyte

Primary Memory V
Prices & Sizes

- Current Numbers (1995)

  64 Million S-R flipflops per chip

  (64M DRAM)

  price = \$50 - \$100 per chip

  64 Mbytes of 8-bit cells with MAR, MDR

  on one card for \$500 -\$800

  Access time = 100 nsec

  About 0.0001 cent per bit

Primary Memory V
Prices & Sizes

- Current Numbers (2001)

256 Million S-R flipflops per chip

(256M DRAM)

price = $50 - $100 per chip

256 Mbytes of 8-bit cells with MAR, MDR

on one card for $500 -$800

Access time = 100 nsec

About 0.00005 cent per bit

Primary Memory V
Prices & Sizes

In prototype:

1 Gigabit DRAM

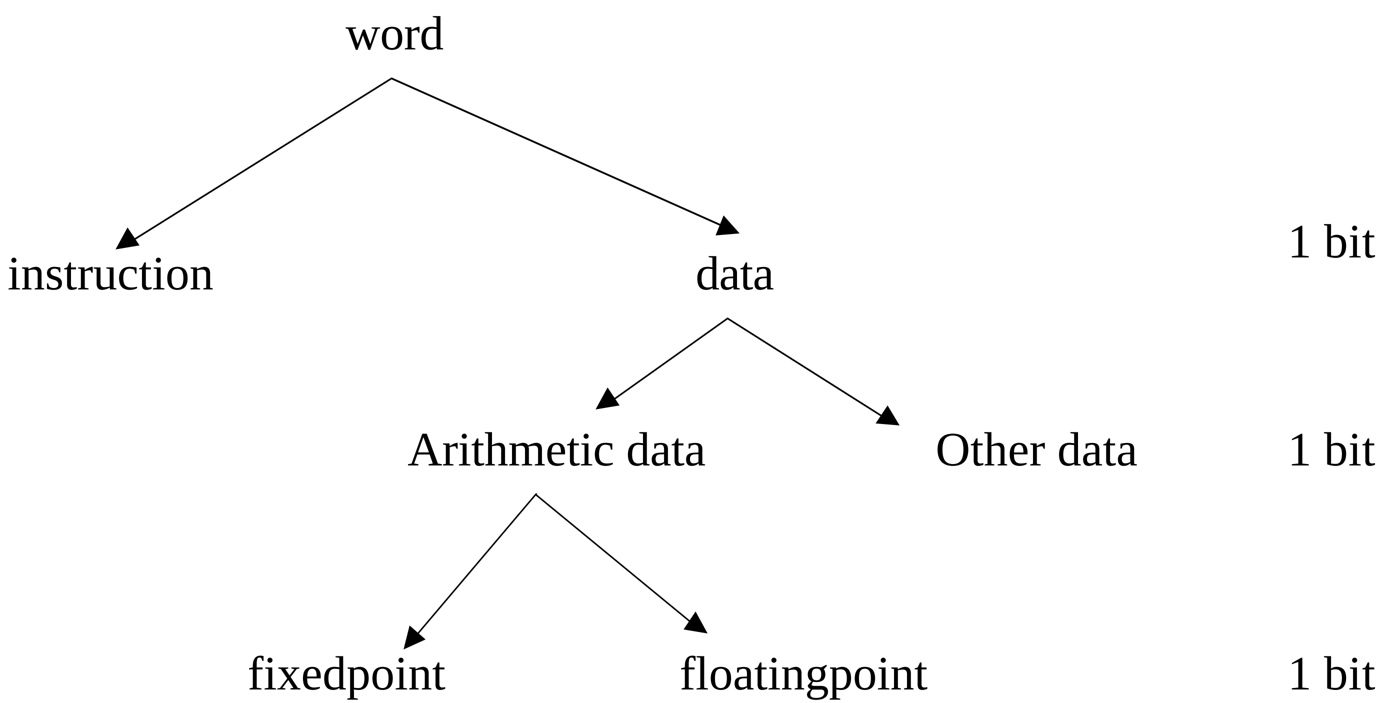
Novel Mp

Metabits:

extra bits per cell
used to specify the *type* of the cell content

typical encoding:

Metabit encoding



Metabits

Used by *tagged architectures*

-data typing in the hardware

PH Lookahead

Look at

Section 7.7

key concept:

historical development of Mp

Mp - Novel
Associative Store or
Content-Addressable memory

Standard memory:

You ask Y??

It answers with c(Y)

CAM:

You ask ‘HELLO’ ??
It responds with Present/Absent. If present,
$\{Y \mid c(Y) = \text{‘HELLO’}\}$

Content-Addressable memory

What for?

Air traffic contrrol

finding cache hits (more later)

updating ROMs