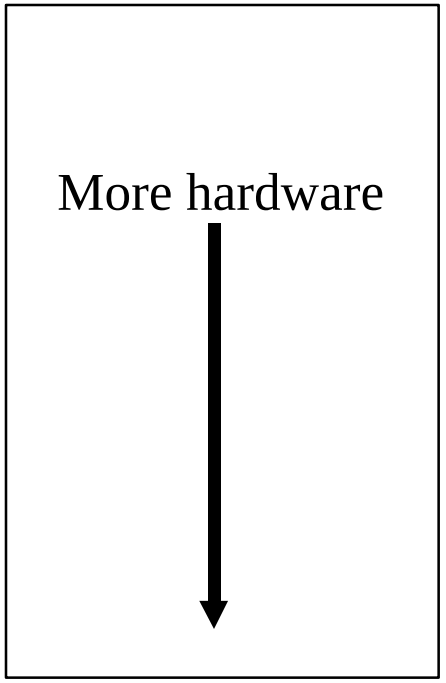
I/O
A Hardware/Software Tradeoff

- Tradeoff Points:

- copy loop
- Direct Memory Access
  - (Block Transfer Controller)
- Channel
- I/O Processor



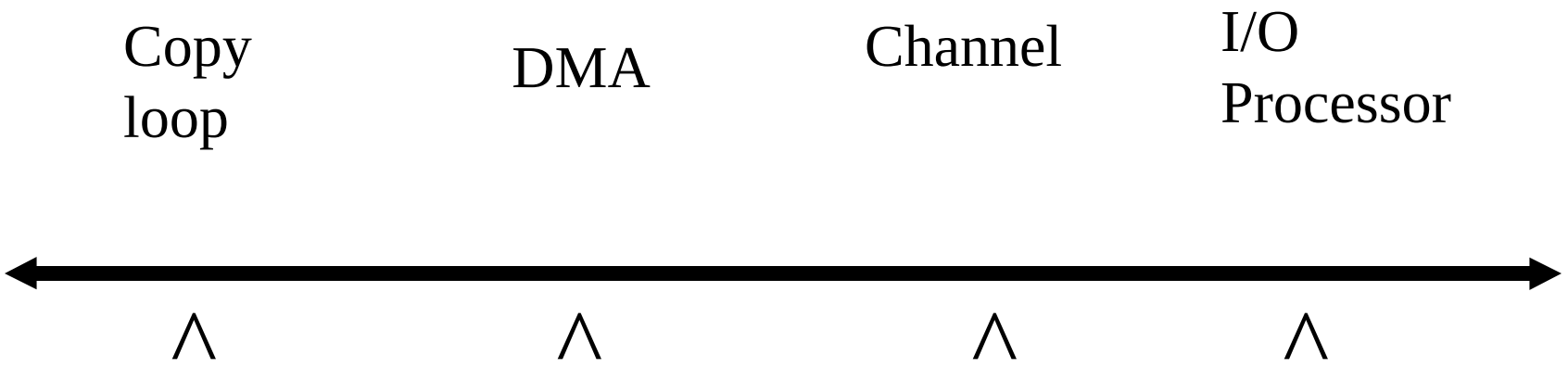
I/O

- The Continuum:

Pure Software  **Pure Hardware**

maximum cpu load — minimum cpu load
minimum hardware cost — maximum hardware cost
worst real time — best real time

I/O



Copy Loop - write

- Send a word
- Wait until Device Ready
- Send another Word

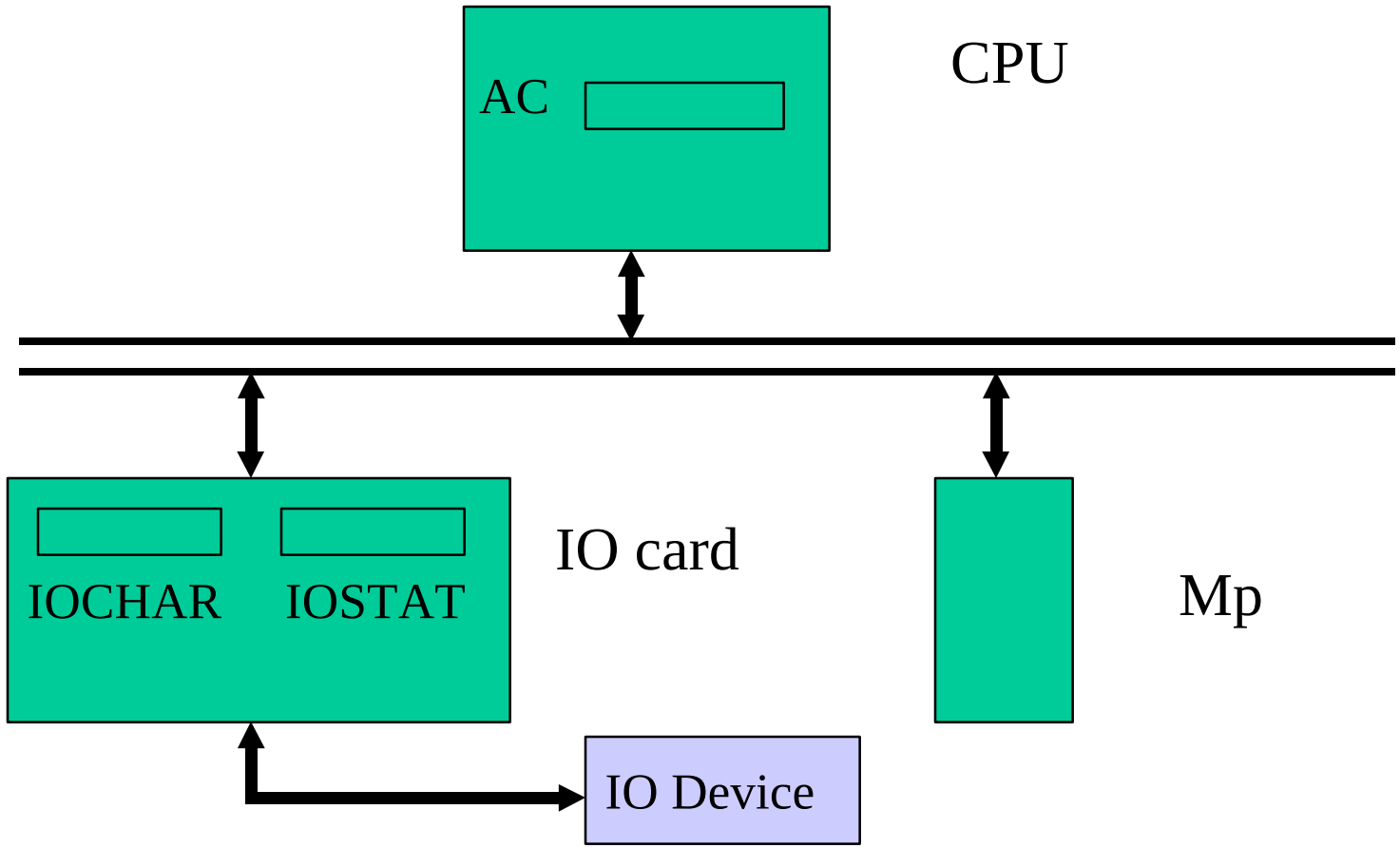
- 99.9% of cpu time wasted!
- Do we care?

```
/* This computer has a write instruction which copies c(register AC)
to an output device. When writing is complete a bit in the I/O status
 and control register is  set .  TST IOSTAT will test the bit; BNRDY
will fail if we're ready.    */

PUTCHAR:   LDA    CHAR;          DATA CHAR TO AC
           WRITE;                WRITE IT OUT
CPYLOOP:   TST    IOSTAT;        DONE YET?
           BNRDY CPYLOOP;        NO
                                 YES, PRINT NEXT CHAR
```

300 BPS TERMINAL: 30 000 μsec/ char versus
2 μsec/ instr or 8 μsec / char !

Copyloop Hardware Support



DMA Controller

- Autonomous block move

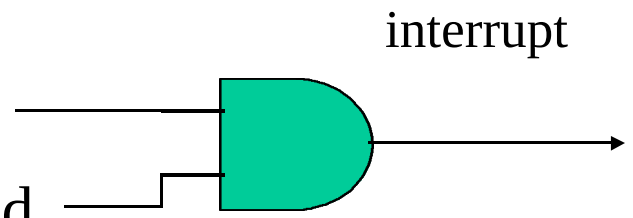
– given start address and byte count

– moves the block of bytes between memory and the device attached to it (read or write)

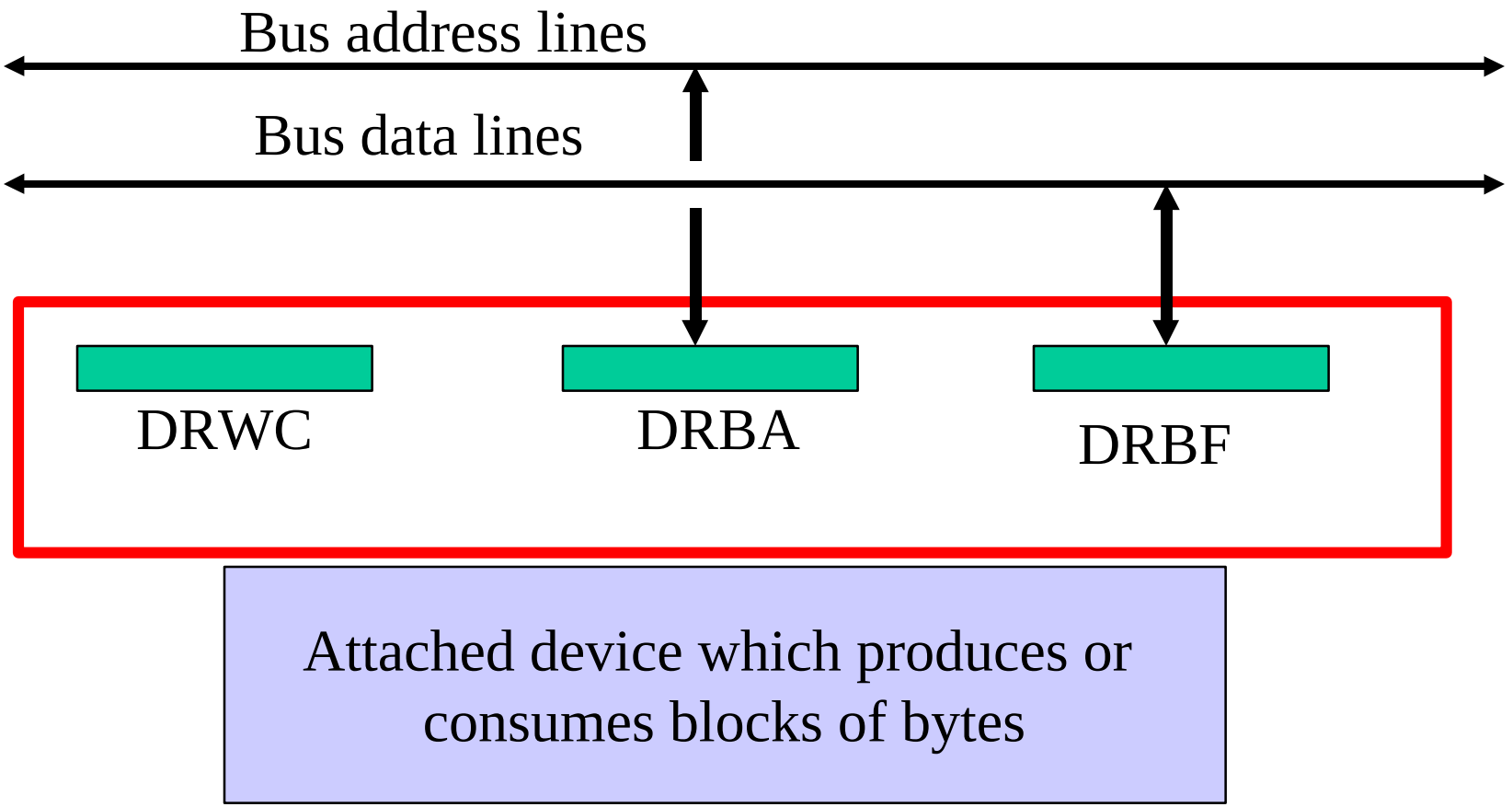
– signals completion by raising an interrupt or setting a bit in its status register

DMA Controller
DEC DR11-B

- DR11-B registers:
  - DRWC: 2's complement of byte count
  - DRBA: bus address = memory address
  - DRBF: byte to be moved
  - DRST: (15) set by error
    - » (7) xfer complete
    - » (6) interrupt enabled
    - » (0) GO



DEC DR11-B
How it works



What it does (memread)

- Seize the bus
- c(DRBA) to bus address lines, assert MEMREAD
- when c(DRBF) is valid, copy to
- when is ready, inc DRWC, DRBA
- if c(DRWC) .NE. 0 GOTO 2. ELSE
- INTERRUPT CPU

Performance

- Cpu runs at full speed except
  - it contends with the DMA device for Mp cycles (and loses one every 30 000 μsec for the case of the 300 bps terminal)
  - attached device runs at full speed or full memory speed, whichever requires fewer Mp cycles/sec

PH Break

- You learn
- pp 565 - 575 (Section 8.5)

Channel

- Stored program controlled device
- can do a sequence of DMA block transfers AND control the attached device (s)
- invented by IBM - /360 architecture

IBM 370 Channel

- 8 24

5 16

IBM 370 Channel

- Channel commands (op codes)
  - WRITE
  - READ
  - READ BACKWARDS
  - CONTROL
  - SENSE
  - TRANSFER IN CHANNEL (BRANCH)

IBM 370 Channel CPU-channel interaction

- Channel Address Word CAW (Channel's program counter) is location 00072 OF MAIN CPU'S MEMORY
- CPU starts channel by executing the CPU INSTRUCTION SIO (start IO)
- Channel can interrupt cpu upon completion of I/O sequence

IBM 370 Channel
What the cpu does

- Store pointer to CCW string in 00072 (CAW)
- execute SIO device_address
- serrvice interrupt when channel is done

Applications

- Multiplexor channel (large number of slow devices, e.g. terminals)

- selector (small number of fast devices, e.g. disc drives)
- scatter write, gather read

Impossibilities

- Formatting
- executing communications protocols
- arithmetic

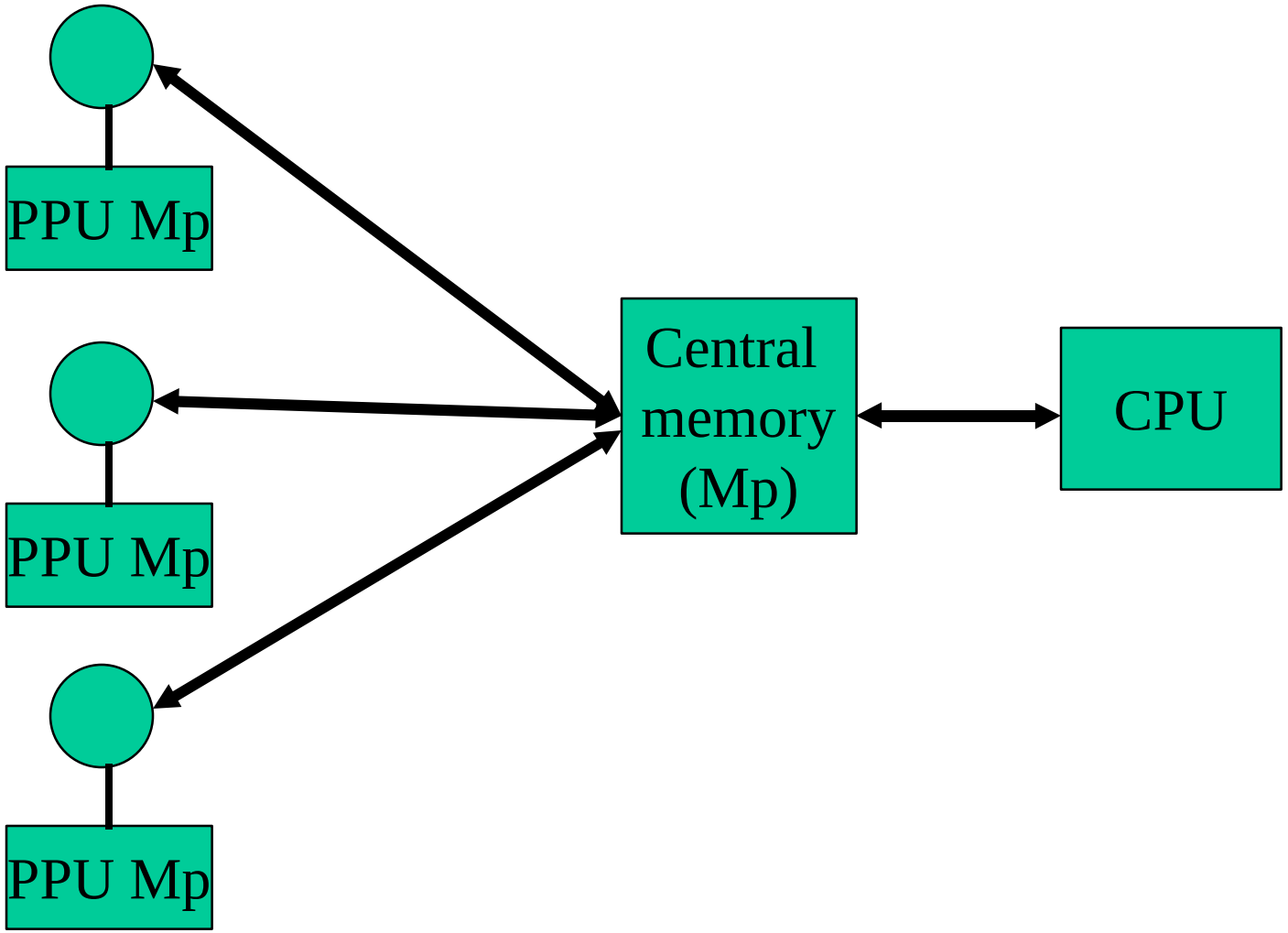
PH Break

- Sections 8.4 - 8.6 of PH Text

I/O Processors
CDC 6600 PPU

-

CDC 6600 PPU



CDC 6600 PPU

- Complete instruction set - a cpu

- 4K words of 12-bit memory
- PPUs do all I/O
- one PPU runs the main cpu operating system (!)

CDC 6600 PPU

PPU - CPU interaction

- PPU can do:
  - CENTRAL MEMORY READ
  - CENTRAL MEMORY

- CPU can do:
  - READ PROGRAM ADDRESS
  - EXCHANGE JUMP