

PUBLICATIONS

D. Michael Miller

**Professor Emeritus
Dept. of Computer Science
University of Victoria
Victoria, BC CANADA**

mmiller@uvic.ca

Books, Contributions to Books

- B1 Hurst, S.L., D.M. Miller and J.C. Muzio. *Spectral Techniques in Digital Logic*, Academic Press, New York & London, 1985.
- B2 Miller, D.M., and J.C. Muzio. "Spectral Techniques for Fault Detection in Combinational Networks" in *Spectral Techniques and Fault Detection*, (M. Karpovsky, editor), Academic Press, London and New York, 1985.
- B3 Miller, D.M. (Editor). *Developments in Integrated Circuit Testing*, Academic Press, New York and London, 1987.
- B4 Miller, D.M. "Integrated Circuit Testing" in *The Encyclopedia of Physical Science and Technology, Yearbook Supplement*, Academic Press, San Diego, 1990.
- B5 Drechsler, R. and D. M. Miller (Guest Editors), "Special Issue: Decision Diagrams," *Multiple Valued Logic: An International Journal*, vol. 4, no. 1-2, 1998.
- B6 Costi, C. and D.M. Miller. "A VHDL Analysis Environment for Design Reuse" in *Virtual Components Design and Reuse*, (Ralf Seepold, editor), Kluwer Academic Publishers, Boston, Nov. 2000.
- B7 Thornton, M.A., R. Drechsler and D.M. Miller. *Spectral Techniques in VLSI CAD*, Kluwer Academic Publishers, The Netherlands, 2001.
- B8 Yanushkevitch, S.N., D.M. Miller, V.P. Shmerko and R.S. Stanković. *Decision Diagram Techniques for Micro- and Nanoelectronic Design*, CRC Taylor & Francis, 2006.
- B9 Miller, D.M., and M.A. Thornton, *Multiple Valued Logic: Concepts and Representations*, Morgan & Claypool, 2008.
- B10 Miller, D.M. and G.W. Dueck, "Translation Techniques for Reversible Circuit Synthesis with Positive and Negative Controls", in *Recent Findings in Boolean Techniques*, (Rolf Drechsler, Daniel Große, editors), Springer, 2021.

Refereed Journal Publications

- J1 De Blonde, G., E.Y. Chuang, B.G. Hogg, D.P. Kerr and D.M. Miller, "Anomalous annihilation of positrons in several solid hydrocarbons," *Can. J. of Physics*, pp. 1619-1622, 1972.

- J2 Miller, D.M., G.E. Miller and D.P. Kerr, "High resolution graphical plotting on a typewriter terminal," *Computer Physics Communications*, pp. 195-197, 1974.
- J3 Muzio, J.C., and D.M. Miller, "Ternary universal decision element," *Notre Dame J. of Formal Logic*, pp. 632-637, 1976.
- J4 Mailer, C., and D.M. Miller, "Saturation transfer electron parametric resonance spectral library," *J. of Magnetic Resonance*, **32**, pp. 289-292, 1978.
- J5 Miller, D.M., and J.C. Muzio, "Detection of symmetries in totally-specified or partially-specified combinational functions," *IEE J. on Computers and Digital Techniques*, **2**, pp. 203-209, 1979.
- J6 Miller, D.M., and J.C. Muzio, "The distribution of symmetry information in the spectrum of a Boolean function," *Electronics Letters*, **15**, pp. 816-817, 1979
- J7 Muzio, J.C., and D.M. Miller, "A class of two-place three-valued unary generators," *Notre Dame J. of Formal Logic*, **21**, pp. 148-154, 1980.
- J8 Miller, D.M., "Spectral addition techniques for many-valued logic functions," *Congressus Numerantium*, **31**, pp. 141-151, 1981.
- J9 Muzio, J.C., D.M. Miller and S.L. Hurst, "Spectral method of Boolean function complexity," *Electronics Letters*, **18**, pp. 572-574, 1982.
- J10 Hurst, S.L., D.M. Miller and J.C. Muzio, "On the number of spectral coefficients necessary to identify a class of Boolean functions," *Electronics Letters*, **18**, pp. 577-578, 1982.
- J11 Muzio, J.C., D.M. Miller and S.L. Hurst, "Multivariable symmetries and their detection," *IEE Proc.*, **130**, pp. 141-148, 1983.
- J12 Eris, E., and D.M. Miller, "Syndrome-testable internally unate combinational networks," *Electronics Letters*, **16**, pp. 637-638, 1983.
- J13 Miller, D.M., and J.C. Muzio, "Spectral fault signatures for internally unate combinational networks," *IEEE Trans. on Computers*, **C-32**, pp. 1058-1062, 1983.
- J14 Miller, D.M., and J.C. Muzio, "Spectral fault signatures for single stuck-at faults in combinational networks," *IEEE Trans. on Computers*, **C-33**, pp. 765-769, 1984.
- J15 Miller, J.C., and D.M. Miller, "Spectral characterization of the self-dualized classification of Boolean functions," *Int. J. Electronics*, **61**, no. 1, pp. 65-72, 1986.
- J16 Bate, J.A., and D.M. Miller, "Exhaustive testing of stuck-open faults in CMOS combinational circuits," *IEE Proc. Pt. E: Computers and Digital Techniques*, **135**, no. 1, pp. 10-16, 1988.
- J17 Hortensius, P.D., R.D. McLeod, W. Pries, D.M. Miller and H.C. Card, "Cellular automata-based pseudorandom number generators for built-in self-test," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, **8**, no. 8, pp. 842-859, 1989.
- J18 Serra, M., T. Slater, J.C. Muzio and D.M. Miller, "Analysis of linear cellular automata and their aliasing properties," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, **9**, pp. 767-778, 1991.

- J19 Zhang, S., D.M. Miller and J.C. Muzio, "Determination of minimal cost linear hybrid one-dimensional cellular automata," *Electronic Letters*, **27**, no. 18, pp. 1625-1627, 1991.
- J20 Tomczuk, R., and D.M. Miller, "Near-optimal PLA input variable pairing using autocorrelation techniques," *Microelectronics J.*, **23**, pp. 523-531, 1992.
- J21 Marcynuk, D.M., and D.M. Miller, "The OR-k method of on-line checking of programmable logic arrays," *J. Electronic Test: Theory and Applications*, **3**, no. 1, pp. 53-66, 1992.
- J22 Walsh, P.A., and D.M. Miller, "Goal-directed simulated annealing and simulated sintering," *Microelectronics J.*, **25**, pp. 363-382, 1994.
- J23 Dubrova, E., D.M. Miller and J.C. Muzio, "Upper bounds on the number of products in AND/OR/XOR expansions of logic functions," *Electronic Letters*, vol. **31**, pp. 541-542, 1995.
- J24 Zhang, S., R. Byrne, J. C. Muzio and D.M. Miller, "Quantitative analysis for linear hybrid cellular automata and LFSR as built-in self-test generators for sequential faults," *J. of Electronic Testing: Theory and Applications*, vol. **7**, pp. 209-221, 1995.
- J25 Miller, D.M., "Function representation and the logic design of digital circuits," *Proc. Information Science Research Group*, Research Institute for Industrial Technique, Kansai University, vol. **10**, no. 3, pp. 23-34, 1996.
- J26 Zhang, S., D.M. Miller and J.C. Muzio, "Notes on complexity of the lookup-table minimization problem for FPGA technology mapping," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. **15**, no. 12, pp. 1588-1590, 1997.
- J27 Dubrova, E., D.M. Miller and J.C. Muzio, "Best ROBDD ordering for functions with disjoint decompositions," *Electronics Letters*, vol. **33**, no. 14, pp. 1198-1200, 1997.
- J28 Miller, D.M., "An improved method for computing a generalized spectral coefficient," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. **17**, No. 3, pp. 233-238, March, 1998.
- J29 Drechsler, R. and D.M. Miller, "Decision diagrams in multi-valued logic," Invited Special Issue Introductory Paper, *Multiple Valued Logic: An International Journal*, vol. **4**, no. 1-2, pp. 1-8, 1998.
- J30 N, Muranaka, T. Murayama, S Imanishi and D.M. Miller, "A quaternary systolic product-sum finite field computation circuit using neuron MOSFETs," *Multiple Valued Logic: An International Journal*, vol. **4**, no. 4, pp. 307-327, 1999.
- J31 Thornton, M. A., and D.M. Miller, "Computation of discrete function Chrestenson spectra using Cayley color graphs," *Journal of Multiple-Valued Logic and Soft Computing*, Special Issue on Spectral Techniques, vol. **10**, no. 2, pp. 189-202, 2004.
- J32 Maslov, D., G.W. Dueck, and D.M. Miller, "Toffoli network synthesis with templates," *IEEE Transactions on Computer Aided Design*, vol. 24, issue 6, pp. 807-817, June 2005.
- J33 Maslov, D., G.W. Dueck, and D.M. Miller. "Two-step synthesis of Toffoli-Fredkin reversible networks," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 13, issue 6, pp. 765-769, June 2005.

- J44 Miller, D.M., D. Maslov, and G.W. Dueck. "Synthesis of quantum multiple-valued circuits," *Journal of Multiple-Valued Logic and Soft Computing*, vol. 12, no. 5-6, pp. 431-450, 2006.
- J45 Maslov, D., and D.M. Miller, "Comparison of the cost metrics through investigation of the relation between optimal NCV and optimal NCT 3-qubit reversible circuits," *IET Computers & Digital Techniques*, vol. 1, number 2, pp. 98-104, March 2007.
- J46 Maslov, D., G.W. Dueck and D.M. Miller and, "Techniques for the synthesis of reversible Toffoli networks," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 12, number 4, pp. 42:1 – 42:28, September 2007.
- J47 Miller, D.M., D. Y. Feinstein and M.A. Thornton, "QMDD minimization using sifting for variable reordering," *Journal of Multiple-Valued Logic and Soft Computing*, vol. 13, number 4-6, pp. 537-552, 2007.
- J48 Maslov, D., G.W. Dueck, D.M. Miller and C. Negrevergne, "Quantum circuit simplification and level compaction," *IEEE Transactions on Computer Aided Design*, vol. 27, number 3, pp. 436-444, March 2008.
- J49 Yamashita, S., S.-i. Minato, and D.M. Miller, "DDMF: An efficient decision diagram structure for design verification of quantum circuits under a practical restriction," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, E91-A(12):3793-3802, 2008.
- J50 Feinstein, D.Y., M.A. Thornton, and D.M. Miller, "Minimization of quantum-multiple-valued decision diagrams using data structure metrics," *Journal of Multiple-Valued Logic and Soft Computing*, vol. 15, no. 4, pp. 361-377, 2009.
- J51 Miller, D.M., and R. Stanković, "A heterogeneous decision diagram package," in *Lecture Notes in Computer Science: Computer Aided Systems Theory - EUROCAST 2009*, Springer, Berlin / Heidelberg, pp. 540-547, 2009.
- J52 Yamashita, S., S.-i. Minato and D.M. Miller, "Synthesis of Semi-classical Quantum Circuits," *Journal of Multiple-Valued Logic and Soft Computing*, vol. 18, no. 1, pp. 99- 114, 2012.
- J53 Miller, D.M., R. Wille and R. Drechsler, "Reducing Reversible Circuit Cost by Adding Lines," *Journal of Multiple-Valued Logic and Soft Computing*, vol. 19, no. -3, pp. 185-201, 2012.
- J54 Sasanian, Z. and D. Michael Miller, "Mapping a Multiple-control Toffoli Gate Cascade to an Elementary Quantum Gate Circuit," *Journal of Multiple-Valued Logic and Soft Computing (MVLSC)*, vol. 18, no. 1, pp. 83-98, 2012.
- J55 Sasanian, Z. and D. Michael Miller, "Transforming MCT Circuits to NCVW Circuits," *Springer's Lecture Notes in Computer Science (LNCS)*, Springer Verlag, vol. 7165, pp. 77-88, 2012.
- J56 Wille, R., D. Grosse, D.M. Miller and R. Drechsler, "Equivalence Checking of Reversible Circuits," *Journal of Multiple-Valued Logic and Soft Computing (MVLSC)*, vol. 19, no. 4, pp. 361-378, 2012.

- J57 Sasanian, Z. and D. M. Miller, "Reversible and quantum circuit optimization: A functional approach," *Springer's Lecture Notes in Computer Science (LNCS)*, Springer Verlag, Vol. 7581, 2012.
- J58 Wille, Robert, Mathias Soeken, D. Michael Miller and Rolf Drechsler, "Trading Off Circuit Lines and Gate Costs in the Synthesis of Reversible Logic," *Integration, the VLSI Journal*, accepted.
- J59 Soeken, Mathias, D. Michael Miller and R. Drechsler, "Quantum circuits employing roots of the Pauli matrices," *Physical Review A*, 88(042322), Pages 042322, 2013.
- J60 Wille, Robert, Mathias Soeken, D. Michael Miller and Rolf Drechsler, "Trading Off Circuit Lines and Gate Costs in the Synthesis of Reversible Logic," *Integration, the VLSI Journal*, Elsevier, Vol. 47, No. 2, 284-294, 2014.
- J61 Soeken, Mathias, Robert Wille, Oliver Keszocze, D. Michael Miller, Rolf Drechsler, "Embedding of Large Boolean Functions for Reversible Logic," *ACM Journal of Emerging Technologies in Computer Systems*, Vol. 12, Issue 4, pp. 41.1 – 41.26, 2015.
- J62 Yamada, C. and D. M. Miller, "Using SPIN to Check Simulink Stateflow Models," *International Journal of Networked and Distributed Computing*, Vol. 4, No. 1, pp. 65-74, 2016.
- J63 Niemann, P., R. Wille, D. M. Miller, and M. A. Thornton, "QMDDs: Efficient Quantum Function Representation and Manipulation," *IEEE Trans. Computer-Aided Design*, Vol. 35, No. 1, 86-99, 2016.
- J64 Miller, D.M. and G.W. Dueck, "Function Translations and Search-based Transformation for MVL Reversible Circuit Synthesis," *Science of Computer Programming*, 25pp., 2021.

Refereed Conference Publications

- C1 Muzio, J.C., and D.M. Miller, "Decomposition of ternary switching functions," *Proc. 3rd Int. Symp. on Multiple-Valued Logic*, pp. 156-165, May 1973.
- C2 Miller, D.M., and J.C. Muzio, "Two-place decomposition of binary functions," *Proc. 3rd Manitoba Conf. Numerical Mathematics*, pp. 293-306, Oct. 1973.
- C3 Miller, D.M., and J.C. Muzio, "A powerful cellular array," *Proc. 3rd Manitoba Conf. Numerical Mathematics*, pp. 315-332, Oct. 1973.
- C4 Miller, D.M., and J.C. Muzio, "A ternary cellular array," *Proc. 4th Int. Symp. on Multiple-Valued Logic*, pp. 469-482, May 1974.
- C5 Miller, D.M., and J.C. Muzio, "A fast method for determining the two-place decompositions of a binary function," *Proc. 4th Manitoba Conf. Numerical Mathematics and Computing*, pp. 293-308, Oct. 1974.
- C6 Miller, D.M., "An algorithm for the chromatic number of a graph," *Proc. 5th Manitoba Conf. Numerical Mathematics and Computing*, pp. 533-548, Oct. 1975.
- C7 Miller, D.M., and J.C. Muzio, "Two-place decomposition and the synthesis of many valued switching functions," *Proc. 6th Int. Symp. on Multiple-Valued Logic*, pp. 164-168, May 1976.

- C8 Miller, D.M., "A canonical representation for many-valued symmetric functions," *Proc. 6th Manitoba Conf. Numerical Mathematics and Computing*, pp. 303-313, Oct. 1976.
- C9 Epstein, G., D.M. Miller and J.C. Muzio "Some preliminary views on the general synthesis of electronic circuits for symmetric and partially symmetric functions," *Proc. 7th Int. Symp. on Multiple-Valued Logic*, pp. 29-34, May 1977.
- C10 Miller, D.M., "A table-driven microprocessor cross-assembler," *Proc. MIMI*, Montreal, pp. 49-55, 1977.
- C11 Muzio, J.C., and D.M. Miller, "On the minimization of many-valued functions," *Proc. 9th Int. Symp. on Multiple-Valued Logic*, pp. 294-299, 1979.
- C12 Miller, D.M., and D.M. Fellows, "Task-structured microprocessor software," *Proc. 1st Can. Workshop on the Design and Development of Computer Systems*, pp. 168-184, May 1979.
- C13 Epstein, G., D.M. Miller and J.C. Muzio, "Selecting don't-care sets for many-valued functions: a pictorial approach using matrices," *Proc. 10th Int. Symp. on Multiple-Valued Logic*, pp. 219-225, June 1980.
- C14 Miller, D.M., "The fanout-free realization of multiple-valued logic functions," *Proc. 11th Int. Symp. on Multiple-Valued Logic*, pp. 246-255, May 1981.
- C15 Miller, D.M., (Invited Address) "Spectral symmetry tests," *Proc. 11th Int. Symp. on Multiple-Valued Logic*, pp. 130-134, May 1981.
- C16 Miller, D.M., (Invited Address) "Recent developments in fault detection," *Congressus Numerantium*, 34, pp. 61-85, 1982.
- C17 Miller, D.M., "The syndrome testing of multiple-valued combinational networks," *Proc. 12th Int. Symp. on Multiple-Valued Logic*, pp. 297-302, May 1982.
- C18 Muzio, J.C., and D.M. Miller, "Spectral techniques for fault detection," *Proc. 12th Int. Symp. on Fault Tolerant Computing*, pp. 152-158, June 1982.
- C19 Muzio, J.C., D.M. Miller and G. Epstein, "The simplification of multiple-valued symmetric functions," *Proc. 13th Int. Symp. on Multiple-Valued Logic*, pp. 111-119, May 1983.
- C20 Miller, D.M., and J.C. Muzio, "Spectral techniques for constrained syndrome testing," *Congressus Numerantium*, 42, pp. 235-250, 1984.
- C21 Bate, J.A., and D.M. Miller, "Fault detection in CMOS circuits and an algorithm for generating Eulerian cycles in directed hypercubes," *Congressus Numerantium*, 47, pp. 107-117, 1985.
- C22 Miller, D.M., "Decomposition technique for the design of internally-unate combinational networks," *Congressus Numerantium*, 51, pp. 217-232, 1985.
- C23 Dueck, G.W., and D.M. Miller, "On the minimization of odd weight functions," *Congressus Numerantium*, 51, pp. 113-122, 1986.
- C24 Miller, D.M., and G.W. Dueck, "A four-valued CCD PLA using the MODSUM," *Proc. 16th Int. Symp. on Multiple-Valued Logic*, 232-241, May 1986.
- C25 Miller, D.M., "Graph algorithms for the manipulation of Boolean functions and their spectra," *Congressus Numerantium*, 57, pp. 177-199, 1987.

- C26 Miller, D.M., and G.W. Dueck, "Direct cover MVL minimization using the truncated SUM operator," *Proc. 17th Int. Symp. on Multiple-Valued Logic*, pp. 221-227, May 1987.
- C27 Miller, D.M., "Directed search minimization of multiple-valued logic functions," *Proc. 18th Int. Symp. on Multiple-Valued Logic*, pp. 218-225, May 1988.
- C28 Liu, V.K., and D.M. Miller, "V & H: a switchbox router," *Can. Conf. on Very Large Scale Integration*, pp. 318-327, Oct. 1988.
- C29 Miller, D.M., "A review of built-in test methodologies," *Can. Conf. on Electrical and Computer Engineering*, Vancouver, Oct. 1988.
- C30 Miller, D.M., "Aliasing analysis of multiple-input data compactors," *Can. Conf. on Electrical and Computer Engineering*, Vancouver, Oct. 1989.
- C31 Zhang, S., and D.M. Miller, "A comparison of LFSR and cellular automata BIST," *Can. Conf. on Very Large Scale Integration*, Ottawa, pp. 8.4.1-8.4.9, Oct. 1990.
- C32 Walsh, P.A., and D.M. Miller, "Single row routing by simulated annealing," *Can. Conf. on Very Large Scale Integration*, Ottawa, pp. 7.4.1-7.4.10, Oct. 1990.
- C33 Dueck, G.W., and D.M. Miller, "RCM-MVL: a recursive consensus MVL minimization algorithm," *Proc. 20 Int. Symp. on Multiple-Valued Logic*, pp. 136-143, May 1990.
- C34 Miller, D.M., S. Zhang, W. Pries and R.D. McLeod, "Estimating aliasing in CA and LFSR based signature registers," *Proc. IEEE ICCAD*, pp. 157-160, 1990.
- C35 Miller, D.M., J.C. Muzio, M. Serra, X. Sun, S. Zhang and R.D. McLeod, (Invited Paper) "Cellular automata techniques for compaction based BIST," *1991 IEEE Int. Symp. on Circuits and Systems*, pp. 1893-1896, 1991.
- C36 Tomczuk, R., and D.M. Miller, "Near-optimal PLA input variable pairing using autocorrelation techniques," *Proc. of Can. Conf. on Very Large Scale Integration*, Kingston, pp. 5.1.1-5.1.9, 1991.
- C37 Walsh, P.A., and D.M. Miller, "Goal directed cooling schedule for simulated annealing," *Proc. of Can. Conf. on Very Large Scale Integration*, Kingston, pp. 6.1.1-6.1.8, 1991.
- C38 Tomczuk, R., and D.M. Miller, "Autocorrelation techniques for multi-bit decoder PLA's," *Proc. 22nd Int. Symp. on Multiple-Valued Logic*, pp. 260-263, May 1992.
- C39 Zhang, S., R. Byrne and D.M. Miller, "BIST generators for sequential faults," *Proc. IEEE ICCD*, pp. 309-317, 1992.
- C40 Tomczuk, R., and D.M. Miller, "Combinational logic synthesis by two-place decomposition and autocorrelation techniques," *Proc of the Can. Conf. on Very Large Scale Integration*, pp. 139-146, Oct. 1992.
- C41 Escalante, M.A., N.J. Dimopoulos, D.M. Miller, K.F. Li and E.G. Manning, "The implementor subsystem in DAME: using OASIS to complete the design automation of microprocessor-based systems," *Proc. of the Can. Conf. on Very Large Scale Integration*, pp. 139-146, 1992.
- C42 Miller, D.M., (Invited Address) "Multiple-valued logic design tools," *Proc. 23rd Int. Symp. on Multiple-Valued Logic*, pp. 2-11, May 1993.

- C43 Muranka, N., S. Imanishi and D.M. Miller, "Decimal addition and subtraction units using the p-valued decimal signed digit number representation," *Proc. 23rd Int. Symp. on Multiple-Valued Logic*, pp. 228-233, May 1993.
- C44 Zhang, S., R. Byrne, J.C. Muzio and D.M. Miller, "Why cellular automata are better than LFSR's as built-in self-test generators for sequential type faults," *Proc. ISCAS*, 1994.
- C45 Miller, D.M., "Spectral transformation of multiple-valued decision diagrams," *Proc. 24th Int. Symp. on Multiple-Valued Logic*, pp. 89-96, May 1994.
- C46 Miller, D.M., "A spectral method for Boolean function matching," *1996 European Design and Test Conf.*, (poster presentation, extended abstract in Proceedings), p. 602, Mar. 1996.
- C47 Miller, D.M., and N. Muranaka, "Multiple-valued decision diagrams with symmetric variable nodes," *Proc. 1996 Int. Symp. on Multiple-Valued Logic*, pp 242-247, May 1996.
- C48 Muranaka, N., S. Arai, S. Iminishi and D.M. Miller, "A ternary systolic product-sum circuit for GF(3^m) using neuron MOSFETs," *Proc. 1996 Int. Symp. on Multiple-Valued Logic*, pp. 92-97, May 1996.
- C49 Drechsler, R. and D.M. Miller, "Implementing a multiple-valued decision diagram package," *Proc. 1998 Int. Symp. on Multiple-Valued Logic*, pp. 52-57, May 1998.
- C50 Nagata, Y., D.M. Miller and M. Mukaidono, "Minimal test set generation for fault diagnosis in R-Valued PLAs," *Proc. 1998 Int. Symposium on Multiple-Valued Logic*, pp. 38-43, May 1998.
- C51 Drechsler, R., and D.M. Miller, "Dual edge operations in reduced ordered binary decision diagrams," *Proc. International Symposium on Circuits and Systems*, pp. 961-964, June 1998.
- C52 Nagata, Y., D.M. Miller and M. Mukaidono, "B-ternary logic based asynchronous micropipelines," *Proc. 1999 Int. Symposium on Multiple-Valued Logic*, pp. 214-219, May 1999.
- C53 Costi, C., and D.M. Miller, "A VHDL analysis environment for design reuse," *Proc. FDL'99 Second International Forum on Design Languages*, 10 pp., published on CD-Rom, August 1999.
- C54 Dubrova, E., P. Everlee, D.M. Miller and J.C. Muzio, "TOP, An algorithm for three-level minimization of PLDs," *Proc. Design, Automation and Test in Europe Conference*, pp. 751, March 2000.
- C55 Nagata, Y., D.M. Miller and M. Mukaidono, "Logic synthesis of controllers for B-ternary asynchronous systems," *Proc. 2000 Int. Symposium on Multiple-Valued Logic*, pp. 402-407, May 2000.
- C56 Costi, C., and D.M. Miller, "A visualization framework for VHDL Analysis," *Fifth Multi-Conference on Systems, Cybernetics and Informatics: Special Session on Modern Digital System Synthesis*, pp. 278-282, Orlando, Fl., July 2001.
- C57 Thornton, M.A., D.M. Miller and W. Townsend, "Chrestenson spectrum computation using Cayley color graphs," *2002 Int. Symposium on Multiple-Valued Logic*, pp. 123-128, May 2002.

- C58 Miller, D.M. and R. Drechsler, "Further Improvements in Implementing MVDDs," *2002 Int. Symposium on Multiple-Valued Logic*, pp. 245-253, May 2002.
- C59 Thornton, M. A., R. Drechsler, and D.M. Miller, "Multi-output timed Shannon circuits," *ISVLSI 2002*.
- C60 Thornton, M. A., R. Drechsler, D.M. Miller and W. Townsend, "Computing Walsh, arithmetic and Reed-Muller Spectral decision diagrams using graph transformations," *GLVLSI 2002*.
- C61 Norris, C. and D.M. Miller, International Conference on Communications in Computing (CIC 2002).
- C62 Miller, D.M., "Spectral and two-place decomposition techniques in reversible logic," *Midwest Symposium on Circuits and Systems*, published on CD-ROM, August 2002.
- C63 Dueck, G.W., D. Maslov, and D.M. Miller, "Transformation-based synthesis of networks of Toffoli/Fredkin gates," *IEEE Canadian Conference on Electrical and Computer Engineering*, Montreal, Quebec, May 2003.
- C64 Miller, D.M., and G.W. Dueck, "On the Size of Multiple-Valued Decision Diagrams," *Proc. 2003 Int. Symposium on Multiple-Valued Logic*, Tokyo, Japan, May 2003, pp. 235-240.
- C65 Miller, D.M., and R. Drechsler, "Augmented sifting of multiple-valued decision diagrams," *Proc. 2003 Int. Symposium on Multiple-Valued Logic*, Tokyo, Japan, May 2003, pp. 275-382.
- C66 Dueck, G.W., D. Maslov, and D.M. Miller, "A transformation-based algorithm for reversible logic synthesis," *IEEE/ACM Design Automation Conference (DAC)*, Anaheim, CA, June 2-6, 2003, pp. 318-323.
- C67 D. Maslov, G. W. Dueck, and D. M. Miller, "Simplification of Toffoli networks via templates", *16th Symposium on Integrated Circuits and System Design*, Sao Paulo, Brazil, September 2003, pp. 53-58.
- C68 D. Maslov, G.W. Dueck, and D.M. Miller, "Fredkin/Toffoli templates for reversible logic synthesis," *International Conference on Computer Aided Design (ICCAD)*, San Jose, CA, November 2003, pp. 256-261
- C69 Miller, D.M., G. Dueck, and D. Maslov, "A synthesis method for MVL reversible logic," *Proc. 2004 Int. Symposium on Multiple-Valued Logic*, Toronto, Canada, May 2004, pp. 74-80.
- C70 Maslov, D., C. Young, D.M. Miller and G.W. Dueck, "Quantum circuit simplification using templates," *2005 Conference on Design and Test Europe (DATE)*, Munich, Germany, March 2005, pp. 1208-1213.
- C71 Maslov, D., D.M. Miller and G.W. Dueck, "Templates for reversible logic synthesis," *PACRIM-2005*, pp. 609-612, Victoria, Canada, August 2005.
- C72 Miller, D.M. and M.A. Thornton, "QMDD: A decision diagram structure for reversible and quantum circuits," *Proc. 2006 Int. Symposium on Multiple-Valued Logic*, Singapore, May 2006, CD, 6 pp.

- C73 Miller, D.M., M.A. Thornton and D. Goodman, "A decision diagram package for reversible and quantum circuit simulation," *Proc. IEEE World Congress on Computational Intelligence*, July 2006, CD, 8 pp.
- C74 Miller, D.M., D.Y. Feinstein and M.A. Thornton, "Variable reordering and sifting for QMDD," *Proc. 2007 Int. Symposium on Multiple-Valued Logic*, Oslo, Norway, May 2007, CD, 7 pages.
- C75 Feinstein, D.Y., M.A. Thornton and D.M. Miller, "Partially redundant logic detection using symbolic equivalence checking in reversible and irreversible logic circuits," *2008 Conference on Design and Test Europe*, pp. 1378-1381, March, 2008.
- C76 Thornton, M.A., D.W. Matula, L. Spenner and D.M. Miller, "Quantum logic implementation of unary arithmetic operations," *Proc. 2008 Int. Symposium on Multiple-Valued Logic*, Dallas, Texas, pp. 202-207, May 2008.
- C77 Feinstein, D.Y., M.A. Thornton and D.M. Miller, "On the data structure metrics of quantum multiple-valued decision diagrams," *Proc. 2008 Int. Symposium on Multiple-Valued Logic*, Dallas, Texas, pp. 138-143, May 2008.
- C78 Yamashita, S., S.-i. Minato and D.M. Miller, "Efficient verification of quantum circuits under a practical restriction," *IEEE 8th International Conference on Computer and Information Technology (CIT2008)*, Sydney, Australia, pp. 873-879, July, 2008.
- C79 Miller, D.M., "Decision diagram techniques for reversible and quantum circuits," *Proc. of 8th Int. Workshop on Boolean Problems*, pp. 1-15, invited address, Sept. 2008.
- C80 Miller, D.M., and M.A. Thornton, "QMDD and spectral transformation of binary and multiple-valued functions," *Proc. of 8th Int. Workshop on Boolean Problems*, pp. 137-144, Sept. 2008.
- C81 Miller, D.M., and R. Stanković, "A heterogeneous decision diagram package," *Extended Abstracts 12th Int. Workshop on Computer Aided Systems Theory (EUROCAST)*, pp. 181-182, Feb. 2009 – 8 pp. extended version accepted for proc., Feb. 2009.
- C82 Wille, R., D. Große, D.M. Miller, and R. Drechsler, "Equivalence checking for reversible circuits," *Proc. 2009 Int. Symp. on Multiple-Valued Logic*, Okinawa, Japan, pp. 324-330, May, 2009.
- C83 Miller, D.M., R. Wille, and G.W. Dueck, "Synthesizing reversible circuits for irreversible functions," *12th EUROMICRO Conf. on Digital System Design*, Patras Greece, pp. 749-756, Aug. 2009.
- C84 Miller, D.M., "Lower cost quantum gate realizations of multiple-control Toffoli gates," *PACRIM-2009*, Victoria, Canada, pp. 308-313, Aug. 2009.
- C85 Wille, R., D.M. Miller and R. Drechsler, "Reducing Reversible Circuit Cost by Adding Lines," *Proc. 2010 Int. Symposium on Multiple-Valued Logic*, Barcelona Spain, pp. 217-222, May, 2010.
- C86 Stanković, S., J. Astola, D.M. Miller and R.S. Stanković, "Heterogeneous Decision Diagrams for Applications in Harmonic Analysis on Finite Non-Abelian Groups," *Proc. 2010 Int. Symposium on Multiple-Valued Logic*, Barcelona Spain, pp. 307-312, May, 2010.

- C87 Miller, D.M. and Z. Sasanian, "Lowering the Quantum Cost of Reversible Circuits," *Midwest Symposium on Circuits and Systems*, pp. 260-263, August 2010.
- C88 Miller, D.M., and Z. Sasanian, "Improving the NCV Realization of Multiple-control Toffoli Gates," *Proceedings of the 9th International Workshop on Boolean Problems*, pp. 37-44, September 2010.
- C89 Miller, D.M., R. Wille and Z. Sasanian, "Elementary Quantum Gate Realizations of Multiple-control Toffoli Gates," *Proc. 2011 Int. Symposium on Multiple-Valued Logic*, pp. 288-293, May 2011.
- C90 Lukac, M., B. Shuai, M. Kameyama, D.M. Miller, "Cache Logic - Using Logical Reversibility to Reduce the CPU-Memory Bottleneck," *Proc. 2011 Int. Symposium on Multiple-Valued Logic*, pp. 131-138, May 2011.
- C91 Sasanian, Z. and D. M. Miller, "NCV Realization of MCT Gates with Mixed Controls," *IEEE Pacific Rim Conference on Communications, Computers and Signal Processing (PACRIM)*, pp. 567-571, 2011.
- C92 Soeken, M., Z. Sasanian, R. Wille, D. M. Miller and R. Drechsler, "Optimizing the Mapping of Reversible Circuits to Four-valued Quantum Gate Circuits," *Proc. 2012 Int. Symposium on Multiple-Valued Logic*, pp. 173-178, 2012.
- C93 Sasanian, Z., R. Wille and D. M. Miller, "Realizing Reversible Circuits Using a New Class of Quantum Gates," *Design Automation Conference (DAC)*, pp. 36-41, June 2012.
- C94 Miller, D.M., M. Soeken and R. Drechsler, "Mapping NCV Circuits to Optimized Clifford+T Circuits," *Fifth Conference on Reversible Computation*, pp. 163-175, July 2014.
- C95 Stanković, Radomir and D. Michael Miller, "Using QMDD in Numerical Methods for Solving Linear Differential Equations via Walsh Functions," *Proc. 2015 Int. Symposium on Multiple-Valued Logic*, 6 pp. 2015.
- C96 Yamada, C., and D. Michael Miller, "Using SPIN to Check Nondeterministic Simulink Stateflow Models," *Proc. 2015 Int. Symposium on Multiple-Valued Logic*, 6 pp. 2015.
- C97 Soeken, M., G. W. Dueck, Md. Mazder Rahman and D. M. Miller, "An Extension of Transformation-based Reversible and Quantum Circuit Synthesis," *Proc. Int. Symp. On Circuits and Systems*, pp. 2290-2293, 2016.
- C98 Soeken, M., G. W. Dueck and D. M. Miller, "A Fast Symbolic Transformation Based Algorithm for Reversible Logic Synthesis," *Seventh Conference on Reversible Computation*, pp. 307-321, 2016.
- C99 Miller, D.M. and M. Soeken, "A Spectral Algorithm for Ternary Function Classification," *Proc. 2018 Int. Symposium on Multiple-Valued Logic*, pp. 198-203 2018.
- C100 Miller D.M. and G.W. Dueck " Search-Based Transformation Synthesis for 3-Valued Reversible Circuits" In: Lanese I., Rawski M. (eds) *Reversible Computation. RC 2020. Lecture Notes in Computer Science*, vol 12227. Springer, pp. 218-236, 2020.
- C101 Miller, D.M. and G.W. Dueck, "A Preliminary Study of Transformation Based Synthesis of Reversible Circuits with Positive and Negative Controls," *Proceedings of the 14th International Workshop on Boolean Problems*, 16 pp., September 2020.

- C102 Smith, K.N., M.A. Thornton and D.M. Miller, "Fast Minimization of Polynomial Decomposition using Fixed-Polarity Pascal Transforms," *Proc. 2020 Int. Symposium on Multiple-Valued Logic*, pp. 259-264, 2020.
- C103 Miller, D.M. and G. W. Dueck, "Descending Order Transformation-based Synthesis of MVL Reversible Circuits," *Proc. 2021 Int. Symposium on Multiple-Valued Logic*, pp. 107-112, 2021.

Other Publications

- O1 Miller, D.M., and D.G. MacNeil, "Algorithm 133, parallel shading of a polygon," *APL Quote-Quad*, **10**, Sept. 1979.
- O2 Miller, D.M., "Spectral techniques for constrained syndrome testing," *Proc. Int. Workshop on Fault Detection and Spectral Techniques*, Boston, Oct. 1983.
- O3 Miller, D.M., "PASSIM: A PASCAL-based digital systems simulator-User's Manual," Dec. 1985.
- O4 Miller, D.M., "On the exhaustive testing of stuck-open faults in CMOS combinational circuits," (with J.A. Bate), *Proc. Technical Workshop: New Directions for IC Testing*, Victoria, Mar. 1986.
- O5 Miller, D.M., "Graph algorithms for the manipulation of Boolean function spectra," *Proc. 2nd Int. Workshop on Spectral Techniques*, Montreal, Oct. 1986.
- O6 Miller, D.M., "A simple switch-level simulation algorithm and its application to stuck-open faults in CMOS circuits," *Proc. 2nd Technical Workshop: New Directions for IC Testing*, Winnipeg, Apr. 1987.
- O7 Miller, D.M., "Channel routing with diagonals," *18th Manitoba Conf. on Numerical Mathematics and Computing*, Sep. 1988.
- O8 Miller, D.M., "Linear cellular automata and LFSRs are isomorphic," *Proc. 3rd Technical Workshop: New Directions for IC Testing*, Halifax, Oct. 1988.
- O9 Miller, D.M., "A study of the fault coverage of LFSR and CA pseudo-random test pattern generators," (with S. Zhang), *Proc. 5th Technical Workshop: New Directions for IC Testing*, Ottawa, Aug. 1991.
- O10 Miller, D.M., "Multi-level synthesis and technology mapping for FPGA's," *Proc. 1st Canadian Workshop on FPGA's*, Winnipeg, June 1993.
- O11 Zhang, Z., R.D. McLeod, D.M. Miller and S. Zhang, "Statistically estimating path delay fault coverage in combinational circuits," *Proc. of IEEE Pacific Rim Conf. on Communications, Computers and Signal Processing*, May 1995 (refereed by short abstract).
- O12 Zhang, S., D.M. Miller and J.C. Muzio, "Quantitative measures of pseudorandom BIST generators and the improvement of delay fault coverage," *Proc. of the 1st IEEE Int. On-Line Testing Workshop*, July 1995.
- O13 Miller, D.M., and F. Kadri, "Enhancing BIST transition fault coverage by TPG output permutation", *Proc. of the 2nd IEEE Int. On-Line Testing Workshop*, July 1996.

- O14 Dubrova, E.V., D.M. Miller and J.C. Muzio, "On the relation between disjunctive decomposition and ROBDD variable ordering," *Proc. of IEEE Pacific Rim Conf. on Communications, Computers and Signal Processing*, pp. 688-691, August 1997 (refereed by short abstract).
- O15 Miller, D.M., and R. Drechsler, "Negation and duality in reduced ordered binary decision diagrams," *Proc. of IEEE Pacific Rim Conf. on Communications, Computers and Signal Processing*, pp. 692-695, August 1997 (refereed by short abstract).
- O16 Dubrova, E.V., and D.M. Miller, "On dependable criteria for dynamic reordering algorithms," *1998 ULSI Workshop*, May 1998.
- O17 Dubrova, E.V., D.M. Miller and J.C. Muzio, "AOXMIN-MV: A heuristic algorithm for AND-OR-XOR minimization," *Proc. 4th International Workshop on Applications of Reed-Muller Expansion in Circuit Design (Reed-Muller 99)*, pp. 37-53, August 1999.
- O18 Dubrova, E.V. and D.M. Miller, "On disjoint covers and ROBDD size," *Proc. of IEEE Pacific Rim Conf. on Communications, Computers and Signal Processing*, pp. 162-164, August 1999 (refereed by short abstract).
- O19 Costi, C. and D.M. Miller, "VALET: An environment to reuse components described in VHDL," *Proc. of IEEE Pacific Rim Conf. on Communications, Computers and Signal Processing*, pp. 297-300, August 1999 (refereed by short abstract).
- O20 Norris, C. and D.M. Miller, "Comparing the performance of IP over ethernet and IEEE-1394 on a Java platform," *IEEE Pacific Rim Conf. on Communications, Computers and Signal Processing*, pp. 481-484, August 2001 (refereed by short abstract).
- O21 Thornton, M. A., D. Michael Miller and R. Drechsler, "Transformations amongst the Walsh, Haar, arithmetic and Reed-Muller spectral domains," *Proc. 4th International Workshop on Applications of Reed-Muller Expansion in Circuit Design (Reed-Muller 2001)*, pp. 215-225, August 2001.
- O22 Miller, D.M., and G.W. Dueck, "Spectral techniques for reversible logic synthesis," *RM-2003 Workshop*, Trier, Germany, March 2003.
- O23 Maslov, D., G.W. Dueck, and D.M. Miller, "Templates for Toffoli network synthesis," *International Workshop on Logic Synthesis*, May 28-30, 2003, pp. 320-326.
- O24 Dueck, G.W., D. Maslov and D.M. Miller, "Transformation-based synthesis of networks of Toffoli/Fredkin gates," *Canadian Conference on Electrical and Computer Engineering*, Montreal, May 4-7, 2003 (refereed by abstract).
- O25 Maslov, D., and D.M. Miller, "Reed-Muller spectra based synthesis of reversible circuits using a quantum cost metric," *Proc. Reed-Muller Workshop*, September 2005.
- O26 Yamashita, S. and D.M. Miller, "Decision diagram data structure to represent quantum circuits," *Institute of Electronics, Communications and Communication Engineers*, November 2006, 6 pp.
- O27 Goodman, D., D.Y. Feinstein, M.A. Thornton and D.M. Miller. "Quantum logic circuit simulation based on the QMDD data structure," *Proceedings of the Workshop on Applications of the Reed-Muller Expansion in Circuit Design and Representations and Methodology of Future Computing Technology (RMW)*, pp. 99-105, May 2007.

- O28 Wille, R., D. Große, D.M. Miller and R. Drechsler, “Equivalence checking of reversible circuits,” *Proc. 12. Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV'09)*, 6 pp., Mar. 2-4, Technische Universität Berlin, 2009.
- O29 Miller, D.M., G.W. Dueck, and R. Wille, “Synthesizing reversible circuits from irreversible specifications using Reed-Muller spectral techniques,” *Proc. Reed-Muller Workshop*, pp. 87-96, May, 2009.
- O30 Sasanian, Z. and D.M. Miller, “Mapping a Multiple-control Toffoli Gate Cascade to an Elementary Quantum Gate Circuit,” *Proc. 2nd Workshop on Reversible Computation*, pp. 83-90, July, 2010.
- O31 Yamashita, S., S.-i. Minato and D.M. Miller, “Synthesis of Semi-classical Quantum Circuits,” *Proc. 2nd Workshop on Reversible Computation*, pp. 93-99, July, 2010.
- O32 Sasanian, Z. and D. M. Miller, “Transforming MCT Circuits to NCVW Circuits,” *Proc. 3rd Workshop on Reversible Computation*, pp. 163–174, 2011.
- O33 Zahra Sasanian, "Realization of Reversible Gates with New Quantum Gate Libraries," *Tagstuhl Seminar on Design of Reversible and Quantum Circuits*, 2011.
- O34 Sasanian, Z. and D. M. Miller, "Reversible and quantum circuit optimization: A functional approach," *Proc. 4th Workshop on Reversible Computation*, pp. 111–122, 2012.
- O35 Miller, D. M., "Synthesis of Linear Nearest Neighbour CNOT Circuits," *2014 Workshop on Post-binary ULSI Systems*, 2014.
- O36 Soeken, Mathias, Michael Kirkedal Thomsen, Gerhard W. Dueck and D. Michael Miller, “Self-Inverse Functions and Palindromic Circuits,” *Proc. Reed-Muller Workshop*, pp. 21-26, May, 2015.
- O37 Thornton, M. A., and D. M. Miller, “On the Computation of Reed-Muller Spectra for Cryptography and Switching Theory Applications,” *Proc. Reed-Muller Workshop*, pp. 21-32, May, 2017.
- O38 Miller, D.M., “Two Function Translations for Reversible Circuit Synthesis,” *2020 Workshop on Post-binary ULSI Systems*, May, 2020.
- O39 Miller, D.M. and G.W. Dueck, “A Preliminary Study of Transformation Based Synthesis of Reversible Circuits with Positive and Negative Controls,” *14th International Workshop on Boolean Problems*, Sept. 2020.

Technical Reports

- T1 Miller, D.M. (with J.C. Muzio), “Compatibility techniques for the decomposition of ternary switching functions,” University of Manitoba Scientific Report #71, 1973.
- T2 Dueck, G.W., and D.M. Miller, “RCM: a recursive consensus minimization algorithm,” University of Victoria Technical Report DCS-148-IR, 1990.
- T3 Marcynuk, D.M., and D.M. Miller, “The OR-k method for on-line checking of programmable logic arrays,” University of Victoria Technical Report DCS-152-IR, 1991.

T4 Marcynuk, D.M., and D.M. Miller, “On the cost of unorderdness in on-line checking schemes for programmable logic arrays,” University of Victoria Technical Report DCS-156-IR.