CSc 360
Operating Systems
Review

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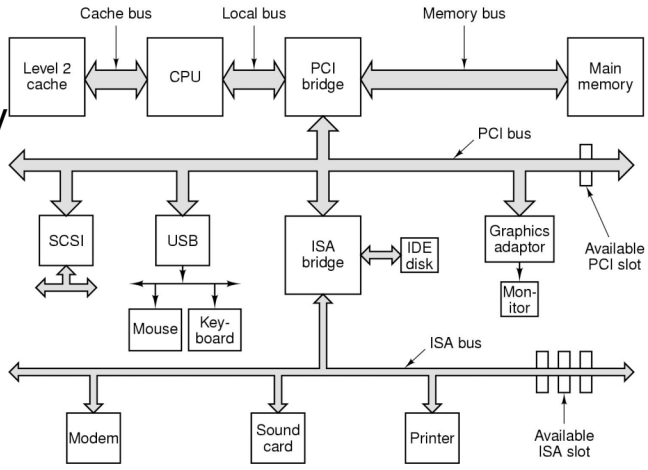
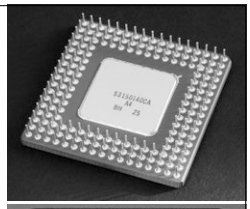
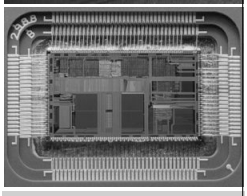
Computer Organization

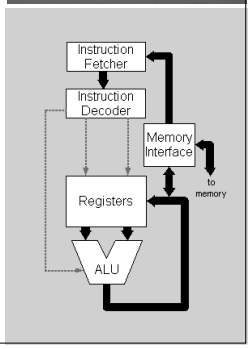
- CPU
- Memory
- I/O



CPU







- Access
  - pins: address, data, control, status
- Internals
  - program counter (PC)
  - registers: address, data, control, flags
  - arithmetic logic unit (ALU), FPU, etc
- Benchmarks
  - clock (GHz), instruction/cycle, MIPS

CPU operations

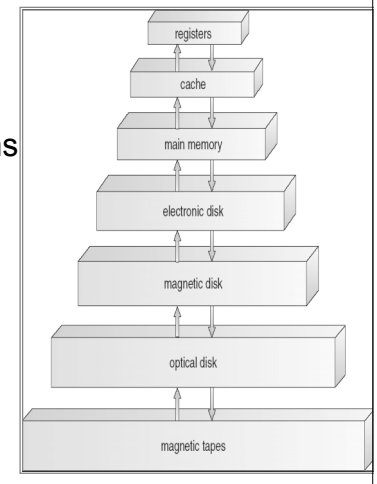
- Fetch
  - retrieve instructions from memory (cache)
- Decode
  - instruction: operator, operands; microcode
- Execute
  - arithmetic/logic operation
  - move data between register, memory, I/O
  - change execution flow

Memory

- Access
  - linear address
  - segmented address: segment, index
  - physical address: cylinder, header, sector (disk)
- Benchmarks
  - clock (MHz)
  - width (bits)
  - throughput (Mbps)

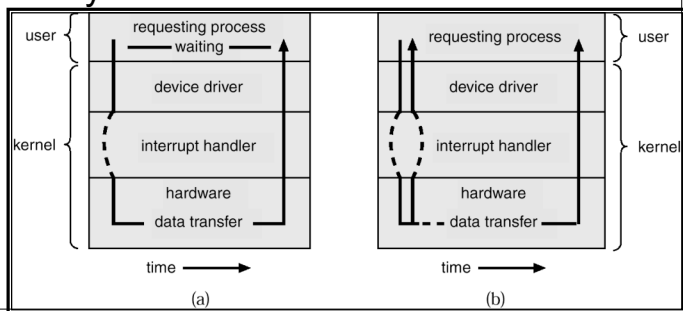
Memory hierarchies

- Speed vs. size (vs. cost)
  - registers: inside CPU
  - cache: transparent to programs
  - memory: main storage
    - DRAM, SDRAM, SRAM, etc
  - disks: secondary storage
    - electronic, magnetic, optical, etc
  - tapes: backup storage
  - networked storage
- Caching



I/O

- A large variety of input/output devices
  - keyboard/mouse, video, audio, network, etc
- Access
  - Address
    - port numbers
    - I/O vs. memory space
  - Interrupt
  - Direct memory access (DMA)
- Synchronous vs asynchronous



Interrupts

- Asynchronous operation
- Nonmaskable interrupts
  - e.g., hardware fault
- Hardware interrupts
  - hardware events: e.g., I/O completion
  - interrupt controller: priority & arbitration
- Software interrupts
  - trap, system call

Interrupt handling

- Save current state
  - CPU counters, registers, flags at system stack
- Update program counter
  - interrupt controller; interrupt vectors
- Execute interrupt routine
- Restore previous state
- Multiple interrupts
  - priority, masking, reentry

DMA

- High-speed I/O, bulk data transfer
- DMA controller
  - source/destination address
  - counter: the amount of data to be moved
- DMA handling
  - program DMA controller
  - execute DMA *concurrently*
  - issue an interrupt on DMA completion

Computer architectures

- Single-processor systems
- Multi-processor systems
  - symmetric multiprocessing (SMP)
- Cluster systems
  - interconnected systems
- Distributed systems
  - networked systems
- Grid systems

This lecture

- Review computer organization and computer architecture
  - CPU, memory, I/O, interrupt, DMA
  - multiprocessor, cluster, distributed, grid
- Explore further
  - Linux with /proc
    - cpuinfo, meminfo, iomem, ioports, interrupts, dma

Next lecture

- An overview on operating systems
  - read OSC Chapter 1